FILE 'INPADOC, HCAPLUS, WPIX, JAPIO' ENTERED AT 10:39:35 ON 28 MAY 2002
L1 1 S 2000KR-0066433/PRN,AP
L2 356 S KIM M?/AU,IN AND PARK S?/IN,AU
L3 13 S L2 AND SAMSUNG?/CS,PA
L4 0 S L3 AND TRENCH ISOLAT#####
L5 0 S L3 AND TRENCH
L6 14 S (KIM M?/AU,IN OR PARK S?/IN,AU) AND SAMSUNG?/CS,PA AND TRENCH
L7 12 S L6 AND ISOLAT#######
L8 0 S L7 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)

FILE 'HCAPLUS' ENTERED AT 10:58:31 ON 28 MAY 2002
L9 3545 S TRENCH(2A)ISOLAT#### OR STI
L10 171 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)
L11 96 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(INTERFACE OR UPPER OR TOP OR REGION OR TRENCH OR ISOLAT######)
L12 29 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(INTERFACE OR UPPER OR TOP)
L13 88 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(TRENCH OR ISOLAT######)
L14 23 S L12 AND L13
L15 67 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)CORNER###
L16 46 S L13 AND L15
L17 15 S L14 AND L15
L18 17 S L12 AND L15
L19 1 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)INTERFACE
L20 29 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(UPPER OR TOP)
L21 11 S L14 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)/TI,IT,ST
L22 0 S L19 NOT L21
L23 727 S (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)INTERFACE
L24 807 S (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)INTERF####
L25 709 S (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)CORNER##
L26 16 S L9 AND (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)SUBSTRATE
L27 866 S (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(TRENCH OR ISOLAT####)
L28 4183 S (CURVE## OR CURVING OR CURVI OR CURVILIN? OR ROUND####)(4A)(LAYER OR FILM)
L29 116 S L10 AND (L23 OR L24 OR L25 OR L26 OR L27 OR L28)
L30 112 S L10 AND (L23 OR L24 OR L25 OR L26 OR L27)
L31 1 S L10 AND L23
L32 1 S L10 AND L24
L33 67 S L10 AND L25
L34 16 S L10 AND L26
L35 88 S L10 AND L27
L36 19 S L10 AND L28
L37 1 S (L31 OR L32)
L38 27 S (L14 OR (L17 OR L18 OR L19 OR L20)) AND L29
L39 16 S L38 NOT (L37 OR L19 OR L21)
L40 171 S L9 AND (L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27 OR L28 OR L29 OR L30 OR L31)
L41 2 S L40 AND BIRD##(W)BEAK
L42 5 S L40 AND BIRD(2W)BEAK
L43 3 S L42 NOT L41
L44 2 S L40 AND THERMAL(W)(OXIDE OR LAYER OR FILM)
L45 3 S L40 AND (SOI OR (SI OR SILICON)(1W)INSULATOR)
L46 3749 S (BURIE## OR BURY####)(W)(LAYER OR OXIDE)
S 7440-21-3/REG#(L)(MONOCRYST? OR MONO CRYST)

FILE 'REGISTRY' ENTERED AT 11:22:25 ON 28 MAY 2002
L47 1 S 7440-21-3/RN

FILE 'HCAPLUS' ENTERED AT 11:22:25 ON 28 MAY 2002
L48 322641 S L47
L49 302 S L48 (L)(MONOCRYST? OR MONO CRYST)
S 7440-21-3/REG#(L)(SINGLE CRYST)

FILE 'REGISTRY' ENTERED AT 11:22:41 ON 28 MAY 2002
L50 1 S 7440-21-3/RN

L1 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:353945 HCAPLUS
TI Trench isolation structure having a curvilinear interface at upper corners of the trench isolation region, and method of manufacturing the same
IN Kim, Min; Park, Sun-hu
PA S. Korea
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L029-00
NCL 257524000
CC 76 (Electric Phenomena)

Published unexamined version of 09/986,247 published 5/9/02

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002053715	A1	20020509	US 2001-986247	20011108 <--
			KR 2000-66433 A	20001109

AB The interface between a trench isolation layer and a semiconductor substrate at the uppermost part of the trench isolation region has a curvilinear sectional profile to prevent an electric field from concentrating at the upper corners of the substrate where the active regions are formed. A pad oxide layer and a hard mask layer are sequentially formed on the semiconductor substrate, and are then patterned using photolithography to form a hard mask pattern and a pad oxide pattern. Subsequently, a thermal oxide layer is formed on the substrate, either directly thereon or in a shallow trench formed therein. The thermal oxide layer and the semiconductor substrate are then etched using the hard mask pattern as a mask to form a deep trench and yet leave an outer peripheral portion of the thermal oxide layer at the upper part of the trench isolation region. A buffer layer is formed over the entire upper stepped surface of the resulting structure and then the deep trench is filled with an oxide layer. The resulting structure is planarized and the hard mask pattern is removed to thereby complete the formation of the trench isolation layer.

L7 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:275691 HCAPLUS
DN 136:317795
TI Semiconductor device having desired gate profile, and semiconductor device fabrication
IN **Kim, Min**; Kim, Sung-Tae
PA **Samsung Electronics Co., Ltd., S. Korea**
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-8247
ICS H01L029-788; H01L029-792; H01L027-115
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002110828	A2	20020412	JP 2001-19189	20010126
PRAI KR 2000-54473	A	20000916		

AB A method for fabricating a semiconductor device, such as a floating-gate semiconductor memory device, having a desired gate profile by a self-aligned shallow **trench isolation** method is described, which involves forming a buffer film such as an oxide or plasma CVD film and an optional antireflection film prior to the **trench** formation. Specifically, the antireflection film may comprise polysilicon, silicon nitride, silicon nitride oxide, and/or silicon oxide.

ST semiconductor device fabrication shallow **trench isolation** buffer antireflection film; memory device fabrication shallow **trench isolation** buffer antireflection film

IT Films
(buffer; semiconductor device having desired gate profile, and semiconductor device fabrication by self-aligned shallow **trench isolation**)

IT Vapor deposition process
(plasma; semiconductor device having desired gate profile, and semiconductor device fabrication by self-aligned shallow **trench isolation**)

IT Antireflective films
Semiconductor device fabrication
Semiconductor devices
Semiconductor memory devices
(semiconductor device having desired gate profile, and semiconductor device fabrication by self-aligned shallow **trench isolation**)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(semiconductor device having desired gate profile, and semiconductor device fabrication by self-aligned shallow **trench isolation**)

IT 7782-44-7, Oxygen, uses 10024-97-2, Nitrogen oxide (N2O), uses
RL: NUU (Other use, unclassified); USES (Uses)
(semiconductor device having desired gate profile, and semiconductor device fabrication by self-aligned shallow **trench isolation**)

Applicant

7 ANSWER 5 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:200000 HCAPLUS
DN 126:286138
TI An experimental high performance 16M DRAM using giga-bit technologies
AU Jeong, Gi-Tae; Cho, Sang-Hyun; **Kim, Min-Jung**; Shin, Yoo-Chul; Kim, Do-Hyung; Jang, Seung-Kyu; Hwang, Bung-Han; Choi, Dong-Uk; Ha, Dae-Won; Kim, Kinam
CS Technology Development, Memory Device Business, **Samsung** Electronics Co., Kyungki-Do, S. Korea
SO ESSDERC'96, Proc. Eur. Solid State Device Res. Conf., 26th (1996), 685-688. Editor(s): Baccarani, Giorgio; Rudan, M. Publisher: Editions Frontieres, Gif-sur-Yvette, Fr.
CODEN: 64CSAW
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB An exptl. high performance 16M DRAM having 0.18 .mu.m design rule for giga bit DRAMs was developed. Junction leakage and junction capacitance was reduced by STI (shallow **trench isolation**). Fast access time even at low operation voltage(.apprx.1.5 V) was achieved by TiSi2 gate, W-bit line, Ta2O5 capacitor, and new circuit techniques. Insufficient depth of focus margin for back-end of line process was overcome by triple metalization scheme with one W and two Al metals. Owing to these, high speed(Trac = 28 ns at 1.5V) and small chip size (5.3x5.4 mm2) was achieved.
ST DRAM exptl high performance; memory device DRAM performance
IT DRAM devices
(exptl. high performance 16M DRAM using giga-bit technologies)
IT 1314-61-0, Tantalum pentoxide
RL: DEV (Device component use); USES (Uses)
(capacitor; exptl. high performance 16M DRAM using giga-bit technologies)
IT 12039-83-7, Titanium disilicide 12039-88-2, Tungsten disilicide
RL: DEV (Device component use); USES (Uses)
(gate; exptl. high performance 16M DRAM using giga-bit technologies)
IT 7429-90-5, Aluminum, uses 7440-33-7, Tungsten, uses
RL: DEV (Device component use); USES (Uses)
(metalization; exptl. high performance 16M DRAM using giga-bit technologies)

Applicant

L39 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:191378 HCAPLUS
DN 130:203821
TI **Trench isolation** method for semiconductor substrate
IN Zheng, Jie; Gabriel, Calvin Todd; Monsees, Suzanne
PA VLSI Technology, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5882982	A	19990316	US 1997-786365	19970116
	US 5939765	A	19990817	US 1997-977645	19971124
	US 6107158	A	20000822	US 1998-47959	19980325
PRAI	US 1997-786365	A3	19970116		

AB A shallow **trench isolation** structure and method for forming such structure. In one embodiment, the semiconductor device isolating structure of the present invention includes a trench formed into a semiconductor substrate. A cross-section of the trench has a 1st sidewall sloping inwardly towards the center of a substantially planar bottom surface, and a 2nd sidewall sloping inwardly towards the center of the substantially planar bottom surface. Addnl., a cross section of the **trench** has a 1st **rounded** bottom **trench corner** at an interface of the 1st sidewall and the substantially planar bottom surface, and a 2nd **rounded** bottom **trench corner** at an interface of the 2nd sidewall and the substantially planar bottom surface. Also, the trench of the present invention has a 1st **rounded upper trench corner** at the interface of the 1st sidewall and the top surface of the semiconductor **substrate**, and a 2nd **rounded upper trench corner** at the interface of the 2nd sidewall and the top surface of the semiconductor substrate. Thus, the trench of the present invention does not have micro-trenches formed into the bottom surface thereof Addnl., the present invention does not have the sharp upper and bottom comers found in conventional trenches formed using a shallow **trench isolation** method. The present invention also provides a method to eliminate deleterious micromasking and spike formation.

IT 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in **trench isolation** method for semiconductor substrate)

L45 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:523203 HCAPLUS
DN 121:123203
TI Method to reduce stress from trench structure on **SOI** wafer
IN Chidambarrao, Dureseti; Hsu, Louis Lu-Chen; Mis, Daniel J.; Peng, James Ping
PA International Business Machines Corp., USA
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 603106	A2	19940622	EP 1993-480199	19931119
	R: DE, FR, GB				
	JP 06216230	A2	19940805	JP 1993-293503	19931124
	JP 2531492	B2	19960904		
	US 5470781	A	19951128	US 1993-166415	19931214
PRAI	US 1992-991010		19921216		

AB In an **isolation trench** in a **Si**-on-**insulator** wafer, the sidewalls of the **trench** **curve** outwardly at the bottom of the trench where the top Si layer meets the underlying oxide insulating layer. A typical **SOI** structure is comprised of a semiconductor substrate, a SiO2 layer, and a single crystal Si layer. A suitable masking oxide layer is deposited on the top surface of the Si layer and a photoresist is formed thereon. The photoresist is developed in the desired trench pattern and an opening for the trench is formed in the oxide mask by means of known semiconductor process steps. An **isolation trench** is formed in the top single crystal Si layer so that its sidewalls at the bottom of the **trench curve** outwardly from the center of the trench. Preferably, the top corners of the **trench** sidewalls are also slightly **rounded** to further reduce points of stress. After the trench is formed, the photoresist is removed and an oxide layer is grown on the trench sidewalls using a conventional process. The trench is then filled with polysilicon using a conventional chem. vapor deposition process. Finally, the structure is planarized. Optionally a stress relief annealing step is carried out at .apprxeq.1050-1100.degree. for .apprxeq.20 min in a forming gas. This sidewall geometry eliminates the sharp corners at the bottom of the trench that are detrimental to device reliability.

ST stress redn trench structure **SOI** wafer
IT Semiconductor devices
(**Silicon**-on-**insulator** wafers for, reducing stress from trench structures on)

L21 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:585346 HCAPLUS
DN 129:224479
TI Use of polymer spacers for the fabrication of shallow **trench isolation** regions with **rounded top** corners
IN Yu, Bo; Zhong, Qing Hua; Ye, Jian Hui; Zhou, Mei Sheng
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5801083	A	19980901	US 1997-954046	19971020

AB A method for forming insulator filled, shallow **trench isolation** regions, with **rounded** corners, has been developed. The process features the use of a polymer coated opening, in an insulator layer, used as a mask to define the shallow trench region in silicon. After completion of the shallow trench formation the polymer spacers are removed, exposing a region of unetched semiconductor, that had been protected by the polymer spacers, during the shallow trench dry etching procedure. The sharp corner, at the intersection between the shallow trench and the unetched region of semiconductor, is then converted to a rounded corner, via thermal oxidn. of exposed silicon surfaces. The polymer spacers also eliminate the top corner wraparound.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(shallow trench formation in semiconductor substrate contg., using polymer spacers)

IT 12033-89-5, Silicon nitride, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(shallow trench formation in semiconductor substrate using polymer spacers)

L39 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:69877 HCAPLUS
DN 130:132685
TI Forming a shallow **trench isolation** structure in a semiconductor body
IN Joyner, Keith
PA Texas Instruments Incorporated, USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438425000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5863827	A	19990126	US 1997-868086	19970603

AB A shallow **trench isolation** (**STI**) is used to isolate 2 active regions from each other. The advantage of **STI** is that the **upper corners** are **rounded**. **Rounding** of the **upper corners** is accomplished using an oxide deglaze prior to sidewall oxidn. of the trench, which undercuts the pad oxide from the pad nitride. The allows the sidewall oxidn. process to form a thicker oxide at the **upper corners**, which in turn **rounds** the **corners**. **Rounded corners** minimize the elec. field strength induced by the geometry. As a result, the Vt lowering that occurs in prior art **STI** structures is minimized and off-state leakage due to the inherent parasitic transistor at the upper corner is reduced.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(forming a shallow **trench isolation** structure in an SOI substrate)

L39 ANSWER 12 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:175642 HCAPLUS
DN 130:190551
TI Shallow **trench isolation** in manufacture of integrated circuits
IN Ho, Michael
PA Winbond Electronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438421000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5880004	A	19990309	US 1997-872255	19970610

AB A method of providing an isolation structure in a semiconductor device having a shallow **trench** with a **rounded top corner** is provided for preventing stress centralization as well as current leakage of a device. The method includes: (a) sequentially forming a pad oxide layer and a Si nitride layer on a semiconductor substrate; (b) forming an opening in the Si nitride layer by a 1st anisotropic etching process, to expose an area for forming a shallow trench; (c) performing a wet etching process to remove the pad oxide layer within the opening, the wet etching process removing a portion of the pad oxide layer extending from the opening and under the Si nitride layer; (d) performing an isotropic etching process to form a hollow with a **rounded top corner** in the semiconductor **substrate**, in which the **rounded top corner** is located under the Si nitride layer; and (e) continuously etching the hollow by a 2nd anisotropic etching process using the Si nitride layer as a mask, thereby forming a shallow **trench** having a **rounded top corner** in the semiconductor substrate.

IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(shallow **trench isolation** in manuf. of integrated circuits contg.)

L21 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:157681 HCAPLUS
DN 132:174576
TI Forming shallow **trench isolation** that has **rounded** and protected corners
IN Yoo, Chue-San; Lee, R. Y.; Tsai, J. H.
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438425000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6033969	A	20000307	US 1996-721758	19960930

AB A method is provided for forming shallow **trench isolation** that has **rounded** and protected corners by 1st forming a bird's beak field oxide layer prior to the trench-forming step such that a **rounded** and protected **top** corner and a **rounded** bottom corner of the **trench** can be formed. The **rounded top** and bottom corners of the shallow trench opening have radii of .gtoreq.100 .ANG. and a trench depth of .ltoreq.5000 .ANG.. The top corner of the trench opening is protected by the beak portion of the bird's beak against etching in a subsequent oxide dip process before gate formation.
IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(forming shallow **trench isolation** having **rounded** and protected corners in manuf. of semiconductor devices contg.)

L21 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:606816 HCAPLUS
DN 133:171122
TI Method for making a **trench isolation** having a conformal liner oxide and **top** and bottom **rounded** corners for integrated circuits
IN Lee, Kuei-ying; Thei, Kong-beng; Chen, Bou-fun
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438400000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6110793	A	20000829	US 1998-104033	19980624

AB A method for forming an improved **trench isolation** having a conformal liner oxide and **rounded top** and bottom corners in the trench was achieved. The conformal liner oxide improves the CVD gap-filling capabilities for these deep submicron wide **trenches**, and the **rounded** corners improve the elec. characteristics of the devices in the adjacent device areas. After etching trenches with vertical sidewalls in the Si substrate, a 2-step oxidn. process is used to form the conformal liner oxide. A 1st oxidn. step using a low-O2 flow rate and a low temp. (.apprx.850-920.degree.) is used to achieve rounded bottom corners. A 2nd oxidn. step at a low-O2 flow rate and a higher temp. (.apprx.1000-1150.degree.) is used to achieve **rounded top** corners. The 2-step process also results in a more conformal liner oxide. The trenches are then filled with a CVD oxide and polished or etched back to an oxidn.-barrier layer/etch-stop layer over the device areas to complete the **trench isolation**.

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for making a **trench isolation** having a conformal liner oxide and **top** and bottom **rounded** corners for integrated circuits)

L21 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:45133 HCAPLUS
DN 134:94400
TI Shallow **trench isolation** method providing **rounded top trench** corners in semiconductor device fabrication
IN Kelley, Patrick J.; Singh, Ranbir; Fritzinger, Larry B.; Lee, Cynthia C.; Molloy, John Simon
PA Lucent Technologies, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438425000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6174786	B1	20010116	US 1999-447154	19991123
PRAI US 1999-115536P	P	19990112		

AB A method of shallow **trench isolation** by forming a trench in a semiconductor device comprises the steps of forming an oxide layer; forming a mask layer; anisotropically etching the mask layer; forming a 2nd oxide layer; forming a cap layer; forming rounded end caps adjacent the mask; and transferring the rounding of the caps to the top corners of the trench. The oxide layer is formed over a substrate of the semiconductor device. The mask layer is formed over the oxide layer. The mask layer is then anisotropically etched to form the mask and an opening in the mask. The opening in the mask exposes the substrate, and the width of the opening is greater than the width of the trench. Blanket etching the cap layer forms the rounded end caps. The rounded end caps are adjacent to the mask on opposite ends of the opening, and the distance between the end caps is about equal to the width of the trench. The trench is formed by plasma etching the trench. During this process, the rounding of the end caps is transferred to the top corners of a trench.

IT 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in shallow **trench isolation** method providing **rounded top trench** corners in semiconductor device fabrication)

L39 ANSWER 2 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:177137 HCAPLUS
DN 136:208885
TI Isolation method of semiconductor device
IN Kim, Dong Chan; Choi, Yeong Ho
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000043241	A	20000715	KR 1998-59591	19981228

AB An isolation method for a semiconductor device is provided to stably form a shallow **trench isolation** structure. A pad oxide and a pad nitride are successively deposited on a semiconductor substrate, and then selectively etched together with the substrate to form a trench into the substrate. After an oxidn. on sidewalls of the trench, an oxide layer is deposited over all surfaces while filling the trench. The oxide layer is then chem. and mech. polished up to the nitride layer, and densified with oxygen atm. and high temp., resulting in **round upper corners** of the **trench**. Next, after the nitride layer is removed, the oxide layer is subjected to an etch-back process using radio frequency plasma. At this time, by increasing pressure of a working gas and shortening mean free path thereof, a shadow effect due to scattering of working gas ions is maximized. Accordingly, an upper edge of the oxide layer is earlier etched than a portion meeting with the pad oxide, and thereby no weak point in morphol. is created.

L39 ANSWER 1 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:241308 HCAPLUS
DN 136:271740
TI Method of fabricating semiconductor device having element **isolation trench**
IN Fujita, Kazunori
PA Sanyo Electric Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L021-8242
ICS H01L021-336; H01L021-331; H01L021-20
NCL 438248000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002037616	A1	20020328	US 2001-960494	20010924
	JP 2002100674	A2	20020405	JP 2000-290163	20000925
PRAI	JP 2000-290163	A	20000925		

AB A method of fabricating a semiconductor device capable of sufficiently **rounding** an opening **upper** end of an element **isolation trench** is obtained. This method of fabricating a semiconductor device comprises steps of forming an element **isolation trench** on a semiconductor substrate, performing thermal oxidn. on at least an opening upper end of the element **isolation trench** while increasing the atm. temp. of the semiconductor substrate beyond a prescribed temp. thereby forming a 1st oxide film and suppressing formation of the 1st oxide film on the opening upper end before the atm. temp. is increased beyond the prescribed temp. The semiconductor substrate is prevented from oxidn. under a low temp., whereby oxidn. is more thickly performed by thermal oxidn. in a high-temp. region while relaxing stress applied to the semiconductor substrate. Oxidn. is thickly performed in the high-temp. region not reducing the oxidizing velocity for a corner portion, whereby the opening upper end of the element **isolation trench** can be sufficiently **rounded**.

L43 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:230908 HCAPLUS
DN 132:341635
TI Active corner engineering in the process integration for shallow **trench isolation**
AU Balasubramanian, N.; Johnson, E.; Peidous, I. V.; Ming-Jr, Shiu; Sundaresan, R.
CS Deep Submicron Integrated Circuits Department, Institute of Microelectronics, Singapore, 117685, Singapore
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2000), 18(2), 700-705
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The elec. characteristics of metal-oxide-semiconductor field effect transistor devices with shallow **trench isolation** (**STI**) were studied to evaluate the active corner shaping and the trench-fill dielec. densification techniques. The suppression of corner parasitic transistor effects was obsd. in the two different corner shaping schemes used. In the 1st approach, an undercut of pad oxide below the nitride mask defining the active region facilitated corner oxidn. during liner oxide growth. In the 2nd approach, a high temp. post-chem. mech. polishing (CMP) oxidn. created a **rounded corner**, forming a mini-**bird's beak** under the nitride mask edge. Cross-sectional TEM shows that, while the post-CMP oxidn. **rounds** the **corner**, the pad oxide undercut produces a concave corner profile. Though both approaches improved the subthreshold characteristics of the transistor, the leakage current of field-edge-intensive diodes became very high for post-CMP oxidn. The leakage was also strongly influenced by the annealing ambient during densification of **STI** gap-fill dielec. An oxidizing ambient resulted in high leakage current whereas a nonoxidizing ambient resulted in low levels of leakage current. The excessive leakage is attributed to the Si defects generated along the **STI** edge as a result of stress exerted by the gap-fill oxide. Densification in nonoxidizing ambient also helped improve the subthreshold characteristics of the transistors with **STI** fabricated using the pad oxide undercut scheme.
IT 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in active corner engineering in process integration for shallow **trench isolation** of MOSFETs)
IT 7631-86-9P, Silica, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses)
(in active corner engineering in process integration for shallow **trench isolation** of MOSFETs)
IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(in active corner engineering in process integration for shallow **trench isolation** of MOSFETs)

L39 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:561631 HCAPLUS
DN 131:164225
TI **Trench isolation** structure for a semiconductor device
IN Parekh, Kunal R.; Li, Li
PA Micron Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-00
NCL 257510000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5945724	A	19990831	US 1998-58404	19980409
	US 6174785	B1	20010116	US 1998-99274	19980618
PRAI	US 1998-58404	A3	19980409		

AB Shallow **trench isolation** regions in a semiconductor device are formed by using sacrificial spacers such as polysilicon spacers having a **rounded** shape to form **trench isolation** areas. The spacer shape is transferred to a semiconductor substrate during an etching process to define the profile of the trench, resulting in a **trench** with substantially **rounded upper** and lower **corners** in the substrate. An oxide filler material is deposited in the trench and over the substrate to form a covering layer. The covering layer is then polished back to form a filled trench region which elec. isolates active areas in the substrate. The polishing step can be performed by a blanket dry etching procedure, or by a combination of chem.-mech. planarization and wet etching. The **rounded** shape of the **trench** improves the elec. characteristics of the trench such that current leakage is decreased, and also provides a more optimized trench profile for filling the trench with the filler material.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; **trench isolation** structure for a semiconductor device using spacers of)

IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**trench isolation** structure for a semiconductor device contg.)

L43 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:193538 HCAPLUS
DN 136:225433
TI Fabrication of semiconductor devices by trenched component isolation in formation of MOS transistors
IN Chishiki, Shigeo
PA Nec Kyushu, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002076109	A2	20020315	JP 2000-253852	20000824

AB The title formation of trenched component isolation in MOS transistors involves (1) patterning a 1st insulator layer and an oxidn.-resistant 2nd insulator layer which are successively provided on a Si substrate, (2) selectively thermal oxidizing the exposed Si substrate surface over the insulator layers as its masks to give a LOCOS oxide film which is formed along the 2nd insulator layer edges with **bird**'s **beaks**, (3) dry etching the LOCOS oxide film and the Si substrate underneath over the 2nd insulator layer as its etching mask to provide grooves, and (4) depositing an insulator film over the entire surface to fill the grooves followed by chem.-mech. polishing the deposited insulator film down to the patterned 2nd insulator layer as a polishing stopper. The groove-filled insulator **layer** is **rounded** on its edges and **bird**'s **beaks** by laser irradn. so as to eliminate humped trench formation and consequently to improve source/drain current-drain voltage characteristics.
IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(amorphous, substrate; fabrication of semiconductor devices by trenched component isolation in formation of MOS transistors)

L151 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:426877 HCAPLUS
DN 131:52788
TI Soft edge induced local oxidation of silicon in forming a semiconductor device isolating structure
IN Haskell, Jake; Laparra, Olivier; Zheng, Jie
PA VLSI Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438425000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5920787	A	19990706	US 1997-783312	19970115

AB A semiconductor device isolating structure and method for forming such a structure. In one embodiment, the semiconductor device isolating structure of the present invention includes a trench formed into a semiconductor substrate. A cross-section of the trench has a 1st sidewall extending to the bottom surface of the trench, and a 2nd sidewall extending to the bottom surface of the trench. Also, the trench of the present invention also has a 1st field **oxide** region formed proximate to the interface of the 1st sidewall and the **top** surface of the semiconductor substrate, and a 2nd field **oxide** region formed proximate to the interface of the 2nd sidewall and the **top** surface of the semiconductor substrate. As a result, the semiconductor substrate has a 1st **rounded corner** formed at the intersection of the **top** surface of semiconductor substrate and the 1st sidewall, and a 2nd **rounded corner** formed at the intersection of the **top** surface of the semiconductor substrate and the 2nd sidewall. In so doing, the present invention eliminates the sharp **upper corners** found in conventional trenches formed using prior art shallow **trench isolation** methods.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent); USES (Uses)
(soft edge induced local oxidn. of silicon in forming semiconductor device isolating structure)

L39 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:423607 HCAPLUS
DN 135:27897
TI **Trench** component **isolation** and semiconductor devices having isolation thereof
IN Park, Tae Shu; Park, Moon Han; Park, Ki Ae; Lee, Han Sin
PA Samsung Electronics Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
ICS H01L021-316; H01L029-78
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001160589	A2	20010612	JP 2000-312495	20001012
	US 6331469	B1	20011218	US 2000-684822	20001010
	DE 10050357	A1	20010628	DE 2000-10050357	20001011
	GB 2360631	A1	20010926	GB 2000-24940	20001011
	CN 1293452	A	20010502	CN 2000-134717	20001012
	US 2001041421	A1	20011115	US 2001-911096	20010723
PRAI	KR 1999-43989	A	19991012		
	US 2000-684822	A3	20001010		

AB The title isolation process involves forming a trench in a nonactive region on a semiconductor substrate, forming a sidewall oxide film (thickness 10-150 .ANG.) by thermal oxidn. on the sidewalls and the bottom of the trench, forming a Si nitride liner on the sidewall oxide thin film, filling the trench over the liner with an insulator material, and etching to remove the top portion of the liner to be recessed. The process gives the **trench upper** edges **rounded** for increased oxidn. in gate insulator film in controlling a hump phenomena caused by field concn. and consequent improved reliability in the devices.

IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(amorphous, insulator film; **trench** component **isolation** and semiconductor devices having isolation thereof)
IT 12033-89-5P, Silicon nitride, properties
RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
(amorphous, liner; **trench** component **isolation** and semiconductor devices having isolation thereof)

L21 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:310544 HCAPLUS
DN 134:319715
TI Method for **STI top rounding** control in semiconductor device manufacture
IN Huang, Tse Yao; Lai, Yun Sen
PA Nanya Technology Corporation, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6225187	B1	20010501	US 1999-283301	19990401
PRAI TW 1999-88102265	A	19990212		

AB This present discloses a method for **STI top rounding** control, the steps comprising: (a) providing a semiconductor substrate; (b) forming an oxide layer on the substrate; (c) forming a hard mask on the oxide layer; (d) forming a photoresist pattern with an opening exposing the hard mask at a predetd. **STI** trench region on the hard mask; (e) etching the exposed hard mask and the underlying oxide layer within the opening in sequence, and continuously over-etching to remove part of the semiconductor substrate to form a window lower than the surface of the oxide layer; and (f) using the photoresist pattern and the hard mask as an etching mask, removing part of the exposed semiconductor substrate in the window to form an **STI** trench.

IT 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, uses
RL: NUU (Other use, unclassified); USES (Uses)
(etching mask; in method for shallow **trench isolation top rounding** control in semiconductor device manuf.)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method for shallow **trench isolation top rounding** control in semiconductor device manuf.)

L21 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:12773 HCAPLUS
DN 134:79749
TI Plasma etching shallow **trench isolation** features for **top rounding** and uniform etch depths in a silicon layer
IN Miller, Alan J.; Vahedi, Vahid
PA Lam Research Corporation, USA
SO PCT Int. Appl., 38 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L021-3065
CC 76-3 (Electric Phenomena)
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001001468	A1	20010104	WO 2000-US17329	20000623
	US 6287974	B1	20010911	US 1999-346563	19990630
	US 6218309	B1	20010417	US 1999-410365	19990930
	EP 1190443	A1	20020327	EP 2000-941674	20000623
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
PRAI	US 1999-346563	A	19990630		
	US 1999-410365	A	19990930		
	WO 2000-US17329	W	20000623		

AB A silicon layer is etched in a plasma processing chamber, and the silicon layer is disposed below a hard mask layer having a plurality of patterned openings. The method includes flowing a first etchant source gas into the plasma processing chamber, forming a first plasma from the first etchant source gas and etching through a first portion of the silicon layer with the first plasma at a first etch rate. The first etch rate being sufficiently slow to form an effective **top-rounded** attribute in a portion of the trench. The method further includes flowing a second etchant source gas into the plasma processing chamber, forming a second plasma from the second etchant source gas and etching through a second portion of the silicon layer with the second plasma, in which the etching with the second plasma extends the trench into the silicon layer without unduly damaging the **top rounded** attribute.

IT 7631-86-9, Silicon oxide, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma etching shallow **trench isolation** features for **top rounding** and uniform etch depths in a silicon layer)

L39 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:555638 HCAPLUS
DN 133:274720
TI An integrated etch approach as **STI** evolves for the 100 nm regime
AU Lassig, Steve; Xu, C. Shan; Miller, Alan J.; Kamath, Sanjay; Romano, Andy; Kudo, Takanori
CS Lam Research Corp., Fremont, CA, USA
SO Solid State Technology (2000), 43(7), 157-158, 160, 162
CODEN: SSTEAP; ISSN: 0038-111X
PB PennWell Publishing Co.
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB As shallow **trench isolation** (**STI**) progresses toward the 100 nm regime, numerous tech. and manufg. problems need to be resolved. The work presented here examines the current process parameter envelope, identifies problem areas, and develops an integration scheme that reduces process complexity and cost. The final scheme includes an integrated etch that could process hard mask opening, **top corner rounding**, and silicon **trench** etch in one pass. It also provides high-d. oxide gap-fill that does not require annealing and can be planarized with direct-polish CMP.
IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(integrated etch approach as shallow **trench isolation** evolves for the 100 nm regime)

L39 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:544877 HCAPLUS
DN 131:293803
TI Roles of sidewall oxidation in the devices with shallow **trench isolation**
AU Pyi, Seung-Ho; Yeo, In-Seok; Weon, Dae-Hee; Kim, Young-Bog; Kim, Hyeon-Soo; Lee, Sahng-Kyoo
CS Semiconductor Advanced Research Division, Hyundai Electronics Industries Company, Ltd., Kyoungki, 467-701, S. Korea
SO IEEE Electron Device Letters (1999), 20(8), 384-386
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The effects of sidewall sacrificial and sidewall oxidns. on the characteristics of devices with shallow **trench isolation** (**STI**) were studied. Sidewall sacrificial and sidewall oxidns. significantly affected junction leakage and gate oxide integrity (GOI). The sidewall sacrificial oxidn. reduces oxidn.-induced stresses and make the **trench top corner** more **rounded** . This reduced stress and more **rounded top corner** led to much improved junction leakage and GOI. These results clearly show that the sidewall sacrificial oxidn. is worth using, although it adds complexity to the **STI** process.
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(sidewall oxidn. effects on properties in devices with shallow **trench isolation**)
IT 7631-86-9P, Silica, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); REM (Removal or disposal); PREP (Preparation); PROC (Process); USES (Uses)
(sidewall oxidn. effects on properties in devices with shallow **trench isolation**)

L21 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:105527 HCAPLUS
DN 132:230205
TI **Round**-off of **trench** corner by post-cylindrical molecular pump sidewall oxidation for 0.25 .mu.m and beyond technologies
AU Chung, Y. S.; Jeon, C. W.; Kim, J. H.; Han, S. K.; Hwang, J. W.; Kim, S. Y.; Lee, J. G.; Hyun, I. S.
CS Bubal-eub, Ami-ri, San 136-1, System IC Research and Development Center, Process Development Laboratory 2, Hyundai Electronics Industries Company Limited, Ichon-si, Kyoungki-do, 467-701, S. Korea
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2000), 18(1), 197-200
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A post-cylindrical mol. pump (CMP) sidewall oxidn. (PCSWO) has been developed for the shallow **trench isolation** (**STI**) process of 0.25 .mu.m and beyond complementary metal-oxide-semiconductor technologies. One of the most important factors of **STI** is a **round**-off of **trench top** corners without the loss of active area. The conventional **STI** process usually requires a wall oxidn. after **trench** etch to **round** off and also an annealing to densify a gap-filled oxide. But PCSWO simplifies the **STI** process by applying sidewall oxidn. and annealing simultaneously. The trench was filled with HDP oxide without the conventional wall oxidn. after trench etch. After CMP, post-CMP wall oxide was thermally grown to **round** off the **trench** corner at the high temp. of 1100.degree.C. The high temp. wall oxidn. has an annealing effect for HDP oxide, which releases a residual film stress. The anomalous subthreshold conduction of the shallow **trench isolated** metal-oxide-semiconductor field effect transistors as the so called "kink effect" due to field crowding at the active edge, was successfully eliminated even at the back bias of .+-.5 V. Isolation and diode characteristics of PCSWO-**STI** were comparable to those of the conventional **STI**. Gate oxide reliabilities of PCSWO-**STI** were similar to those of the conventional **STI**.
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(**round**-off of **trench** corner by post-cylindrical mol. pump sidewall oxidn. for 0.25 .mu.m and beyond technologies)
IT 7631-86-9P, Silica, uses
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(**round**-off of **trench** corner by post-cylindrical mol. pump sidewall oxidn. for 0.25 .mu.m and beyond technologies)

L21 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:782176 HCAPLUS
DN 132:159466
TI Stress minimization of corner **rounding** process during **STI**
AU Olsen, Christopher S.; Nouri, Faran; Rubin, Mark E.; Laparra, Olivier; Scott, Gregory S.
CS VLSI Technology, Inc., San Jose, CA, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3881(Microelectronic Device Technology III), 215-223
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB For sub 0.25 .mu.m CMOS processes, Shallow **Trench Isolation** (**STI**) is required because of its planarity, high packing d. and low junction edge capacitance. After trench etch in the **STI** process, the top corner of the **trench** must be **rounded** in order to achieve stable device performance, reduce inverse narrow width effects and maintain good gate oxide integrity. Several methods of **round** in the **trench** corners have been proposed. A post-CMP oxidn. step to **round** the **top** corner **trench** has been shown to consume too much of the silicon active area and may not be suitable for sub-0.18 .mu.m technologies. Furthermore, the post-CMP oxidn. can generate a lot of stress even at high temps. It has been shown that a 50 nm radius of curvature provides stable device data and a good gate oxide integrity with min. consumption of the active area. In this paper, we have shown that this radius can be achieved with minimal stress generation using a properly optimized rapid thermal oxidn. before oxide fill. Through both 2D oxidn. modeling and exptl. verification we have shown that an optimum oxidn. temp. can be found when coupled with an undercut of the buffer oxide under the silicon nitride mask. Temp. is the primary parameter for **rounding** of the **top** corner during oxidn. while undercut of the buffer oxide lowers the min. temp. for a given rounding. A 50 nm radius of curvature can be achieved by the balance of the two parameters. This radius of curvature has been shown to suitable for 0.15 .mu.m technol. and beyond.
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(stress minimization of corner **rounding** process during shallow **trench isolation** in CMOS device fabrication)

L41 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:748270 HCAPLUS
DN 131:345329
TI Shallow **trench isolation** of MOSFETs with reduced corner parasitic currents
IN Peidous, Igor V.
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8224
NCL 438436000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5989978	A	19991123	US 1998-116610	19980716

AB A method is described for forming MOSFETs with shallow **trench isolation** wherein the abrupt corners introduced by anisotropically etching the silicon trenches are modified by an oxidn. step which **rounds** off the **corners** and also reduces the effect of tensile stresses caused by the densified trench filler material. The method selectively exposes the corner regions to an oxidn. whereby the formation of an oxide **birds-beak** modulates the corners and introduces a compressive stress component in the corner region. Several variations of the procedure are disclosed, including embodiments wherein **birds-beaks** extending in both a vertical and horizontal directions from the corners are employed. The channel and gate oxide edges of MOSFETs extend to these corners. By attenuating the abrupt corners and reducing the mech. stresses, gate oxide integrity is improved and anomalous sub-threshold currents of MOSFETs formed are abated.
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(shallow **trench isolation** of MOSFETs with reduced corner parasitic currents)

L21 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:537478 HCAPLUS
DN 135:115556
TI **Top** corner **rounding** for shallow **trench** **isolation** in semiconductor devices
IN Chiu, Hsien-Kuang; Chen, Fang-Cheng; Tao, Hun-Jan
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-302
ICS H01L021-425
NCL 438711000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6265317	B1	20010724	US 2001-756529	20010109

AB A process for **top**-corner **rounding** at the rim of shallow trenches used for **STI** is described. This is achieved by 1st forming the trench using a Si nitride hard mask having a layer of pad oxide between itself and the Si surface. The Si nitride is then briefly and selectively etched so that it pulls back from over the trench rim and exposes a small amt. of the underlying pad oxide. Rounding by means of sputtering is then effected with the pad oxide serving to protect the underlying Si until just before rounding takes place. The result is smoothly rounded corners free of facets and overhangs.

IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(**top** corner **rounding** for shallow **trench** **isolation** in semiconductor devices)

L151 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:794287 HCAPLUS
DN 132:29651
TI Forming a shallow **trench isolation** structure
IN Lin, Chih-Hung; Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438433000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6001707	A	19991214	US 1999-241760	19990201
	TW 406350	B	20000921	TW 1998-87120246	19981207
PRAI	TW 1998-87120246	A	19981207		

AB A method for forming a shallow **trench isolation** structure in a substrate includes forming a doped region around the future **top corner** regions of a trench. The concn. of dopants inside the doped region increases toward the substrate surface. Thereafter, a trench is formed in the substrate, and then **thermal** oxidn. is carried out. Using the higher oxidn. rate for the doped substrate relative to undoped regions, the **upper corners** of the trench become **rounded corners**. Subsequently, a liner **oxide** layer is formed over the substrate surface inside the trench using conventional methods. Finally, insulating material is deposited in the trench to form a **trench isolation** structure.

L39 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:886810 HCAPLUS
DN 136:14243
TI Semiconductor apparatus with **trench isolation** and method for fabricating the same
IN Kawada, Shinzi; Kawano, Hiroyuki
PA Japan
SO U.S. Pat. Appl. Publ., 23 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L021-76
NCL 438430000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001049178	A1	20011206	US 2001-864201	20010525
	JP 2001345375	A2	20011214	JP 2000-161928	20000531
PRAI	JP 2000-161928	A	20000531		

AB First, a substrate, on which a plurality of semiconductor devices is formed, is provided. Next, a 1st etching treatment is carried out to the substrate with a 1st etching gas comprising CF4 to form a base **trench** having a **rounded**-off **upper** edge or tapered upper edge. A 2nd etching treatment is carried out to the substrate to form a trench region at the base trench so that the **trench** region has a **rounded**-off **upper** edge. And then, an insulating layer is formed on the substrate to fill up the trench region therewith.

IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor app. with **trench isolation** and method for fabricating same)

L151 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:794285 HCAPLUS
DN 132:29649
TI Method of fabricating a shallow **trench isolation** by using **oxide**/oxynitride layers
IN Cheng, Hsu-Li; Jeng, Erik S.; Lin, Wei-Ray
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
ICS H01L021-425
NCL 438410000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6001704	A	19991214	US 1998-90720	19980604

AB A stacked layer including a 1st **oxide**, a nitride layer, a 2nd **oxide** layer, and an oxynitride layer is formed on the **top** of the 1st **oxide** layer. The oxynitride, the 2nd **oxide**, and the nitride are etched through a photoresist. **Oxide** spacers are formed on the sidewalls of the pattern structure, and the oxynitride layer is removed during the formation of the **oxide** spacers. Trenches are generated by a dry etching technique. The 2nd **oxide** and the **oxide** spacers are removed. Next, **thermal** oxidn. is performed to **round** the **corners** of the trench openings. A gap filling material is deposited in the trenches and formed on the nitride. Next, chem. mech. polishing (CMP) is used to remove the **top** of the CVD **oxide** and the nitride layer. The residual nitride layer, the CVD **oxide**, and the pad **oxide** are removed to create **trench isolation** structures with **rounded corners**.

IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes 132614-63-2, Silicon nitride **oxide** (Si(N,O))
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(prepg. shallow **trench isolation** by using **oxide**/oxynitride layers)

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(prepg. shallow **trench isolation** for semiconductor devices contg.)

L39 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:151512 HCAPLUS
DN 136:192801
TI Process for forming a shallow **trench isolation** by etching nitride layers
IN Yu, Shiuh-Sheng; Lee, Chun-Hung; Liang, Ming-Chung
PA Macronix International Co., Ltd., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6350660	B1	20020226	US 2001-840896	20010425

AB First of all, a semiconductor substrate that has a pad oxide layer thereon is provided. Then a nitride layer is formed on the pad oxide layer. Next, a photoresist layer is formed and defined on the nitride layer. Afterward, performing a residual etching process to etch the nitride layer to form an opening and a convex remainder of the nitride layer. The convex remainder of the nitride layer and the semiconductor substrate are then etched by way of using a **top rounding** process to form the **rounding corners** on the semiconductor **substrate**. Subsequently, performing a process for forming the trench to form a **trench** with the **rounding corners**. Finally, the follow-up processes were performed to form the shallow **trench isolation**.
IT Nitrides
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(process for forming shallow **trench isolation** by etching nitride layers)

L39 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:416655 HCAPLUS
DN 135:13124
TI Semiconductor devices having **trench** component **isolations** and conductor patterns and fabrication thereof
IN Koike, Masahiro
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
ICS H01L027-08; H01L029-78
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001156165	A2	20010608	JP 1999-339555	19991130

AB The title fabrication involves forming **trench** component **isolations** on a Si **substrate**, sputtering to **round** the **top** of the projected portion of the **trench** component **isolation** regions, and patterning conductors such as gate electrode in the active regions **isolated** from the **trench** component **isolation** regions. The process prevents residual presence around the **trench** component **isolation** regions and avoids consequent short circuiting which is caused by the residues thereof.

IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(amorphous, substrate; semiconductor devices having **trench** component **isolations** and conductor patterns and fabrication thereof)

IT 12033-89-5P, Silicon nitride, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses)
(etching stopper; semiconductor devices having **trench** component **isolations** and conductor patterns and fabrication thereof)

IT 7631-86-9P, Silica, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses)
(pad oxide film; semiconductor devices having **trench** component **isolations** and conductor patterns and fabrication thereof)

L44 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:31867 HCAPLUS
DN 136:94570
TI Shallow **trench isolation** type semiconductor device
IN Lee, Keum-joo; Park, Tai-su; Kwon, Young-min; Moon, Bong-ho; Hwang, In-seak; Song, Chang-lyoung
PA S. Korea
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L029-00
NCL 257510000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002003275	A1	20020110	US 2001-899224	20010706
	JP 2002043409	A2	20020208	JP 2001-126211	20010424
PRAI	KR 2000-39319	A	20000710		

AB A shallow trench type (**STI**) type semiconductor device employs an etch-stop layer pull-pack approach and a liner as an O barrier, enhancing stability of gate insulation and reliability of transistor operation, in which a trench sidewall **thermal oxide** layer with a thickness of 20 .ANG.-140 .ANG. is formed between Si substrate and the liner, controlling the sidewall liner tension that acts on the substrate. This makes it possible to control the thickness of a gate insulating layer adjacent to a trench to a value equal to or greater than a value in the middle of an active region. Further, a corner adjacent to the **trench** is **rounded** to increase the voltage handling capability of device.

IT 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(oxygen barrier liner; shallow **trench isolation** type semiconductor device)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(substrate; shallow **trench isolation** type semiconductor device)

L45 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:882055 HCAPLUS
DN 136:14170
TI Manufacture of **trench-isolated** semiconductor devices on **SOI** wafers
IN Ito, Satoru
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001338975	A2	20011207	JP 2000-159869	20000530

AB The **SOI** wafers comprise support substrates, insulator films and semiconductor layers on the top. The **trench** structure comprises **isolation trenches** penetrating the semiconductor layers, insulator films on the sidewalls of the semiconductor layers, and isolation insulator films filling the trenches, where the semiconductor layer edge at the **trenches** is **rounded**. Trench formation involves etching and thermal oxidn. Break down and redn. of withstand voltage of gate insulator films are prevented.

L43 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:728178 HCAPLUS
DN 136:13585
TI Optimization of active area edge protection in shallow **trench isolation**
AU Augendre, E.; Rooyackers, R.; Pochet, S.; Grau, L.; Sleeckx, E.; Vandamme, E. P.; Badenes, G.
CS IMEC, Louvain, B-3001, Belg.
SO Proceedings - Electrochemical Society (2001), 2001-2(ULSI Process Integration II), 539-546
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB Because of its higher scalability, Shallow **Trench Isolation** (**STI**) is mandatory for deep sub-micron technologies. Amongst most crit. issues of **STI** is the optimization of trench top corners to preserve device off-state current and reliability. Possible solns. include a nitride guard ring or a **bird's beak**, at the cost of topog. or elec. width. In addn., technologies using std. **STI** processes need careful tuning to avoid the post-filling reoxidn. of trench sidewall that can generate defects. To address these issues, we investigated the innovative sealing of trench sidewalls with a thin oxide/nitride stack to reduce gate wraparound and block post-filling reoxidn. while preserving trench scalability and gate-level topog. The implementation of this approach in 0.18 .mu.m technol. shows that corner optimization requires both wraparound suppression and **corner rounding**.

L21 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:660676 HCAPLUS
DN 127:325399
TI Formation of an **isolation trench** with **rounded top** edges using an etch buffer layer
IN Ho, Chin-hsiung; Tsai, Chia-shiung; Liu, Cheng-kai; Tsai, Chaochieh
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 437067000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5674775	A	19971007	US 1997-803466	19970220

AB The **rounded top** edges give a gate oxide with a uniform thickness around the trench, thereby reducing parasitic field FET problems. The method begins by forming a pad layer over a semiconductor substrate. Next, an insulating layer composed of Si nitride is formed over the pad layer. A 1st opening is formed in the insulating layer and the pad layer, exposing the surface of the substrate. The 1st opening is defined by sidewalls of the pad layer and of the insulating layer. An etch buffer layer composed of polysilicon is formed over the resultant surface. In 1 etch step, the etch buffer layer is anisotropically etched, forming spacers on the sidewalls of the pad layer and of the insulating layer. The same etch step continues by etching the spacers and the exposed substrate in the 1st opening, thereby forming a trench in the substrate. Because the etch has to etch through the spacers before it reaches the substrate, the **trench** has **rounded top** edges near the pad layer. Lastly, the pad layer and the 1st insulating layer are removed, thereby forming the **trench** with **rounded top** edges.

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(formation of **isolation trench** with **rounded top** edges using etch buffer layer in semiconductor devices contg.)

L39 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:566377 HCAPLUS
DN 127:255987
TI Correlation between gate oxide reliability and the profile of the trench top corner in shallow **trench isolation** (**STI**)
AU Park, Tai-su; Shin, Yu Gyun; Lee, Han Sin; Park, Moon Han; Kwon, Sang Dong; Kang, Ho Kyu; Koh, Young Bum; Lee, Moon Yong
CS Semiconductor R&D Cent., Samsung Electronics Co., Ltd., Kyungki-Do, 449-900, S. Korea
SO Tech. Dig. - Int. Electron Devices Meet. (1996) 747-750
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB To develop a Shallow **Trench Isolation** (**STI**) which does not have trench corner induced degrdn. of the gate oxide, its integrities were evaluated with **rounded**, non-**rounded** **top corner**, and an addn. of the CVD SiO2 spacer. In the expt., the **rounded** and SiO2 spacered **STI** showed the best result meaning no harmful influence of the corner to the gate oxide integrity. Also, etch-back processes of the filled CVD SiO2 were modified to eliminate the degrdn. of the gate oxide by a stress concn. at top corner kinks.
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(correlation between gate oxide reliability and profile of etched trench top corner in shallow **trench isolation**)
IT 7631-86-9, Silica, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(correlation between gate oxide reliability and profile of etched trench top corner in shallow **trench isolation**)

L39 ANSWER 15 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:197849 HCAPLUS
DN 114:197849
TI Manufacture of MOS semiconductor device
IN Hieda, Katsuhiko
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L029-784
ICS H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02260660	A2	19901023	JP 1989-83507	19890331

AB Methods are described for manufg. a MOS semiconductor device with an improved cut-off property. The methods involve forming element-**isolation trenches** having **round top** positions.
ST MOS semiconductor device isolation
IT Transistors
(MOS, manuf. of, isolation region formation in)

L39 ANSWER 16 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:34294 HCAPLUS
DN 114:34294
TI Manufacture of semiconductor devices
IN Fukuda, Hisashi; Okabe, Yutaka
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02174139	A2	19900705	JP 1988-325920	19881226

AB The title process comprises formation of side walls in an opening of a mask layer on a semiconductor substrate, etching of the semiconductor substrate to form a groove for isolation, further widening of the upper portion of the groove by removal of the side wall film and etching of the semiconductor substrate, formation of an insulating film on the inner wall in the groove, and filling of the groove with polycryst. Si and of the upper portion of the groove with an insulating film. A device **isolation** groove has **rounded** steps at its **top**, a SiO2 film side wall and a channel-cut layer doped with B+ in p-Si substrate under its bottom, and penetrates a n+-buried layer in the Si substrate. The concn. of stress at the top of the Si layer in the groove was alleviated.

IT 7440-21-3, Silicon, uses and miscellaneous
RL: USES (Uses)
(semiconductor devices with top widened **trench isolation** filled with)

IT 7631-86-9, Silica, uses and miscellaneous
RL: USES (Uses)
(semiconductor devices with **trench isolation** of side walls from)

L151 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:603227 HCAPLUS
TI Method for fabricating a shallow-**trench isolation** structure with a **rounded corner** in integrated circuit
IN Huang, Kuo-tai; Yang, Gwo-shii; Yew, Tri-rung; Lur, Water
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5956598	A	19990921	US 1998-164736	19981001
	US 6087262	A	20000711	US 1998-189140	19981109
PRAI	TW 1998-87110706	A	19980702		

AB A semiconductor fabrication method is provided for fabricating a shallow-**trench isolation** (**STI**) structure with a **rounded corner** in integrated circuits through a rapid **thermal** process (RTP). In the fabrication of the **STI** structure, a sharp **corner** is often undesirably formed. This sharp **corner** , if not eliminated, causes the occurrence of a leakage current when the resultant IC device is in operation that significantly degrades the performance of the resultant IC device. To eliminate this sharp **corner** , an RTP is performed at a temperature of above 1,100.degree. C., which temperature is higher than the glass transition temperature of the substrate, for about 1 to 2 minutes. The result is that the surface of the substrate is oxidized into an sacrificial **oxide** layer and the sharp **corner** is deformed into a **rounded** shape with a larger convex radius of curvature. This allows the problems arising from the existence of the sharp **corner** to be substantially eliminated. Compared to the prior art, this method not only is more simplified in process, but also allows a considerable saving in **thermal** budget, which makes this method more cost-effective to implement than the prior art.

L151 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:132729 HCAPLUS
DN 130:244861
TI In-situ nitride mask open
AU Williams, Scott
CS Silicon Etch Division, Applied Materials, Inc., Sunnyvale, CA, 94086, USA
SO IEEE/CPMT International Electronics Manufacturing Technology Symposium, 23rd, Austin, Tex., Oct. 19-21, 1998 (1998), 146-149 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 67HHAB
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB As feature size approaches 0.25.box.m and below, shallow **trench isolation** (**STI**) has become the most favorable isolation scheme. One challenge in the development of a prodn.-worthy **STI** process is to combine the hard mask open and **STI** step into a single etch chamber. An **STI** process with an in situ hard mask open will provide lower cost of ownership as well as higher throughput. Chamber cleanliness is another crit. issue for **STI** processes using conventional etchants of HBr, Cl2, and O2. HBr related etch byproducts usually result in severe deposition inside the chamber, thus causing particle problems. This paper describes a nitride mask open process using a clean fluorine-based chem. which was successfully integrated into an **STI** process. However, the aggressive nature of the fluorine-based chem. also attacks the photoresist and tends to etch the nitride isotropically. Therefore, it is essential to choose process parameters that maximize the selectivity to photoresist and yield the most vertical nitride etch. Source power, bias power, gas flow, and pressure were all studied to maximize process performance. A typical sample consisted of an 8" silicon wafer with 25 nm of **thermally** grown **oxide**, 200 nm of nitride, and a 700. nm DUV photoresist mask. SEM micrographs were used to monitor the effects on profile angle, **corner rounding**, selectivity, and microloading. Quartz crystal monitor data and a 1000 wafer burn in both indicate that there is no deposition on the dome chamber walls.
IT Nitrides
RL: TEM (Technical or engineered material use); USES (Uses)
(shallow **trench isolation** process with in-situ nitride mask)

L73 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:646273 HCAPLUS
DN 133:231441
TI **Trench isolation** for electrically active components
IN Uhlig, Ines; Zimmermann, Jens; Wege, Stephan
PA Infineon Technologies A.-G., Germany
SO PCT Int. Appl., 20 pp.
CODEN: PIXXD2
DT Patent
LA German
IC ICM H01L021-762
ICS H01L021-3065
CC 76-3 (Electric Phenomena)
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2000054326	A1	20000914	WO 2000-DE716	20000307
W: CN, JP, KR, US				
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
DE 19910886	A1	20000928	DE 1999-19910886	19990311
PRAI DE 1999-19910886	A	19990311		

AB The invention relates to a **trench isolation** for elec. active components, esp. a flat **trench isolation** (shallow **trench isolation**) in e.g. **cryst. Si**, and to a method for producing such a **trench isolation**. The aim of the invention is to reduce stress-related voltages. According to the invention, the junction between the **trenches** of the **isolation** and the side walls is **rounded** and is addnl. provided with tapered side walls so that the angle between the bottom and the side walls is 75><la<190>.

IT 12033-89-5, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**trench isolation** for elec. active components)

L73 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:359761 HCAPLUS
DN 130:360151
TI Ion implantation process to improve the gate oxide quality at the edge of a shallow **trench isolation** structure
IN Fulford, H. Jim; May, Charles E.
PA Advanced Micro Devices, Inc., USA
SO PCT Int. Appl., 18 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L021-762
ICS H01L021-316
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9927578	A1	19990603	WO 1998-US10179	19980518
	US 5915195	A	19990622	US 1997-977795	19971125
	EP 1034565	A1	20000913	EP 1998-923504	19980518
	R: DE, FR, GB, NL				
	JP 2001524752	T2	20011204	JP 2000-522621	19980518
PRAI	US 1997-977795	A	19971125		
	WO 1998-US10179	W	19980518		

AB A semiconductor fabrication process comprising forming a dielec. on an upper surface of a single **crystal Si** substrate. A trench mask is then patterned on an upper surface of the dielec. The trench mask exposes portions of the dielec. situation over portions of the isolation region. Exposed portions of the dielec. are then removed and portions of the Si within the isolation are also removed to form an **isolation trench** within the Si substrate. This formation gave corners in the Si substrate where the upper surface of the Si substrate intersects with sidewalls of the **isolation trench**. Localized damage is then created in regions proximal to these corners of the Si substrate preferably through the use of one or more ion implantation processes performed at implant angles .gtorsim.30.degree.. During the subsequent formation of a liner oxide on the sidewalls and floor of the **isolation trench**, the localized damage region results in a higher oxidn. rate of the Si substrate proximal to the Si substrate corners. This higher oxidn. rate results in a **rounding** or smoothing of the Si corners thereby resulting in a less severe gradient between the Si active region and the **isolation trench**.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(ion implantation process to improve gate oxide quality at edge of shallow **trench isolation** structure)

L74 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:238226 HCAPLUS
DN 136:271688
TI Semiconductor devices having **trench isolation** system and fabrication of device thereof
IN Taniguchi, Arihiro
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
ICS H01L021-28; H01L021-762; H01L021-3205
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002093900	A2	20020329	JP 2000-278326	20000913

AB The title fabrication involves forming an oxide film and a Si nitride film successively on a Si substrate, providing a trenched groove to the substrate over the patterned Si nitride film as a mask, filling the trench with an oxide film, surface leveling down to expose the Si nitride film, removing the oxide and the Si nitride film, and providing a sidewall oxide film to the step formed around the **buried oxide** film. The formation of the **rounded** sidewalls to the oxide step makes removal of excess polycryst. Si deposition easy and smooth without trace of residues in latter process.
IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(amorphous, substrate, trenched isolation formation; semiconductor devices having **trench isolation** system and fabrication of device thereof)

L85 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:828095 HCAPLUS
DN 135:337902
TI Method for manufacturing a **trench isolation**
IN Hwang, Doo Hyun; Gu, Bon Young; Kim, Byung Gi; Nam, Seok Woo
PA Samsung Electronics Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000007971	A	20000207	KR 1998-27586	19980709

AB The invention relates to a process for making **isolation trenches** semiconductor integrated circuit device, comprising the steps of: forming a trench etching mask on a semiconductor substrate; forming a trench by partially etching the semiconductor substrate using the trench etching mask; and forming an oxide layer at both sidewalls and a bottom portion of the trench using a **high temp.** oxidn. of 1000 .degree.C more than, thereby **rounding** the edge of the trench. The **high temp.** oxidn. step further comprises the sub-steps of loading the semiconductor substrate into the chamber.
ST **trench isolation** etching mask integrated circuit
IT Etching masks
Integrated circuits
(**trench isolation** of semiconductor integrated circuit device)

L85 ANSWER 5 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:362954 HCAPLUS
DN 133:11651
TI Semiconductor devices with shallow **groove isolation** (SGI) structures and their manufacture
IN Ishizuka, Norio; Miura, Hideo; Ikeda, Shuji; Yoshida, Yasuko; Suzuki, Norio; Funabashi, Norimasa
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000150630	A2	20000530	JP 1998-317777	19981109
	US 6284625	B1	20010904	US 1999-434308	19991105
	US 6326255	B1	20011204	US 2000-675053	20000929
PRAI	JP 1998-317777	A	19981109		
	US 1999-434308	A3	19991105		

AB The devices are manufd. by (1) formation of .gtoreq.5 nm-thick pad oxide layer on a semiconductor substrate, (2) formation of a oxidn.-prevention layer thereon, (3) formation of a groove using the oxidn.-prevention layer as a mask, (4) setback (e.g. 10 .+-. 5 nm from the edge) of the pad oxide layer, (5) dry oxidn. (H2/O2 .apprxeq. 0) of the formed groove, under conditions satisfying 0 < C .ltoreq. 0.88t - 924 [C(%) is the partial pressure in air, t(.degree.) is the oxidn. temp.], (6) filling the oxidized groove with an insulating layer, (7) removal of the insulating layer formed on the oxidn.-prevention layer, (8) removal of the oxidn.-preventing layer formed on the circuit-forming face of the substrate, and (9) removal of the pad oxide layer on the circuit-forming face. Devices manufd. by the above process are also claimed. The groove edges can be made **round** even under thin pad oxide conditions.

IT 12033-89-5, Silicon nitride, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(oxidn.-preventing layer in; formation of **round** groove edges in manuf. of semiconductor devices having shallow **groove isolation** structure)

L85 ANSWER 6 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:369980 HCAPLUS
DN 130:360175
TI Trench edge **rounding** method and structure for **trench isolation** in device fabrication
IN Jang, Wen-yueh
PA Winbond Electronics Corporation, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438425000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5910018	A	19990608	US 1997-803844	19970224

AB The present invention provides a method to achieve shallow **trench isolation** (**STI**) on the quarter-micron scale. A thin oxide layer, a thick nitride layer, a thick oxide layer and a thin nitride layer are formed sequentially on a Si substrate. A photoresist (PR) layer is then applied as a mask for the isolation regions. The top nitride layer, the top oxide layer and the bottom nitride layer are then etched away from the areas not covered by the PR layer. The PR layer is then removed. An isotropic oxide etch is then applied to create a recess along the bottom oxide layer. A thin oxide layer is then grown on the exposed Si surface. A thin nitride layer is then deposited to fill the recess in the bottom oxide layer. An anisotropic nitride etch is applied to form a nitride spacer along the isolation edge. A thick oxide layer is then grown and removed. This step is repeated as necessary to obtain the desired trench slope. The Si substrate is then etched to a predetd. depth using the oxide and nitride layers as a hard mask. The top nitride layer is also etched away. After the trench is etched, the top oxide layer is removed and thermal oxidn. is applied. The trench sidewalls are then doped using implantation and/or thermal diffusion to enhance device isolation. The trench is then filled with oxide using a CVD (Chem. Vapor Deposition) process. **High temp**. annealing is then applied to increase the integrity of the CVD oxide film. The CVD oxide layer is then polished using CMP (Chem. Mech. Polishing). The nitride layer is then removed. CMP or oxide etchback is then used to planarize the Si surface.

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(trench edge **rounding** method and structure for **trench isolation** in device fabrication)

L85 ANSWER 7 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:329969 HCAPLUS
DN 130:345978
TI Method for **rounding** and thickening the corners of **isolating trenches** formed in semiconductor bodies with a planar surface by using disposable spacer and trench oxidation
IN Wang, Larry Y.
PA Advanced Micro Devices, Inc, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM C03C015-00
NCL 438444000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5904543	A	19990518	US 1996-623632	19960328

AB The method comprises a first step of forming a masking material on the planar surface. Edges of the masking material are offset from the corners of the **isolating trenches**. The second step includes growing an oxide on an exposed portion of the substrate under **high temp**. The oxidn. under **high temp**. causes the corners of the **isolating trenches** to become **rounded**.

IT 12033-89-5, Silicon nitride, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(CVD and etching of silicon nitride on silicon oxide grown on a semiconductor planar surface and then etching it)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(substrate for **rounding** and thickening corners of **isolating trenches** formed in semiconductor bodies with a planar surface by using disposable spacer and trench oxidn.)

L85 ANSWER 8 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:160874 HCAPLUS
DN 130:274657
TI Novel corner **rounding** process for shallow **trench isolation** utilizing MSTS (Micro-Structure Transformation of Silicon)
AU Matsuda, S.; Sato, T.; Yoshimura, H.; Takegawa, Y.; Sudo, A.; Mizushima, I.; Tsunashima, Y.; Toyoshima, Y.
CS Microelectronics Engineering Laboratory, Yokohama, 235-8522, Japan
SO Technical Digest - International Electron Devices Meeting (1998) 137-140
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A new **STI** (Shallow **Trench Isolation**) corner **rounding** technique with MSTS (Micro-Structure Transformation of Silicon) which utilizes Si-migration phenomenon with hydrogen ambient annealing [1] is proposed and applied to 0.15 .mu.m CMOS technol. Highly controlled corner **rounding** radius is achieved without **high temp**. oxidn. process. Thus it is free from defect generation and undesirable impurity diffusion in Si substrate. Subthreshold current due to parasitic corner transistors of the **STI** structure is effectively suppressed and the reverse narrow channel effect is controlled down to 0.2 .mu.m channel width.
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(shallow **trench isolation** utilizing microstructure transformation of Si)

L85 ANSWER 9 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:285466 HCAPLUS
DN 129:34923
TI A highly manufacturable corner **rounding** solution for 0.18 .mu.m shallow **trench isolation**
AU Chang, C. P.; Pai, C. S.; Baumann, F. H.; Liu, C. T.; Rafferty, C. S.; Pinto, M. R.; Lloyd, E. J.; Bude, M.; Klemens, F. P.; Miner, J. F.; Cheung, K. P.; Colonell, J. I.; Lai, W. Y. C.; Vaidya, H.; Hillenius, S. J.; Liu, R. C.; Clemens, J. T.
CS Bell Laboratories, Lucent Technologies, Murray Hill, NJ, 07974, USA
SO Technical Digest - International Electron Devices Meeting (1997) 661-664
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB In this Work, the authors 1st establish the relation between corner leakage and corner **rounding** through device simulation. Then, the authors demonstrate a novel method to produce corner **rounding**, using a post-CMP, **high temp**. reoxidn. process (HTR-**STI**). A semi-empirical model correlating **rounding** with reoxidn. and nitride mask thickness is derived from mech. studies. Finally, the authors show the elec. properties of devices with HTR-**STI** for the 0.18 .mu.m technol.
IT 12033-89-5, Silicon nitride, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(mask; method for producing corner **rounding** in device fabrication)
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(method for producing corner **rounding** in device fabrication)

L85 ANSWER 11 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:114548 HCAPLUS
DN 118:114548
TI Manufacture of silicon substrate isolated with dielectric
IN Imura, Makoto; Kusakabe, Kenji
PA Japan Silicon Co., Ltd., Japan; Mitsubishi Materials Corp.; Mitsubishi Electric Corp.
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04188648	A2	19920707	JP 1990-315081	19901119

AB The method involves (1) anisotropically etching a 1st single-crystal Si substrate to form element-**isolation grooves**; (2) isotopically etching the edges of the groove to obtain **round** and smooth edges; (3) filling the grooves with a polycryst. Si layer after forming an oxide film; (4) polishing the Si layer to obtain a smooth surface; (5) joining a 2nd single-crystal Si substrate to the smooth surface; and (6) polishing the 1st substrate to expose the grooves and to form lands isolated with the oxide film.
IT 7440-21-3, Silicon, uses
RL: USES (Uses)
(oxide isolation of)

L85 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:420589 HCAPLUS
DN 83:20589
TI Optimization of the hydrazine-water solution for anisotropic etching of silicon in integrated circuit technology
AU Declercq, Michel J.; Gerzberg, Levy; Meindl, James D.
CS Stanford Electron. Lab., Stanford Univ., Stanford, Calif., USA
SO J. Electrochem. Soc. (1975), 122(4), 545-52
CODEN: JESOAN
DT Journal
LA English
CC 76-13 (Electric Phenomena)
AB Anisotropic etching of Si with the N2H4-H2O mixt. is studied and characterized for its practical use in integrated circuit technol. The soln. is applied to {100} wafers where the etch presents a V-shaped cross section limited at the side walls by {111} planes and at the bottom by a {100} plane. The etching process is evaluated in terms of the etch rate of the {100} plane, quality of side walls and bottom surface, and corner **rounding**. The results are both concn. and temp. dependent. The optimal temp. for the etching process is 100.degree. for both simple temp. control and high quality etching. The optimal mixt. concn. must be chosen according to the particular use of the anisotropic etching. The optimal vol. concns. of N2H4 for the various applications are: 65% for V-metal-oxide-semiconductor devices and for V-**groove isolation** rings, 70-80% for 2-level structures with flat bottom surface, and for electrode and sensor fabrication.

L87 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:223680 HCAPLUS
DN 136:225313
TI Method for forming **isolation** layer of **trench** structure of semiconductor device
IN Jung, I. Seon
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000045908	A	20000725	KR 1998-62528	19981230

AB A method for forming device isolation layer of a trench structure of a semiconductor device is applied to reduce humps by dispersing elec. field along with **round** shape of a trench edge. A method for forming a device isolation layer of a trench structure of a semiconductor device includes following steps. At the 1st step, a pad oxide layer and a nitride layer are accumulated sequentially on a semiconductor substrate. At the 2nd step, a trench is formed in the semiconductor substrate by etching the lower portion of the substrate with a device isolation mask process and an etching process. At the 3rd step, an oxide layer is **buried** in the trench and the oxide layer is flattened so as to be lower than the nitride layer. At the 4th step, the edge portion of the trench is formed to be **round** by performing the oxidn. process at the temp. at 900-1200.degree.. At the 5th step, the nitride layer is removed, and an rinsing process is performed.
IT 16833-27-5, Oxide 18851-77-9, Nitride
RL: DEV (Device component use); USES (Uses)
(layer of; method for forming **isolation** layer of **trench** structure of semiconductor device)

L87 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:125517 HCAPLUS
DN 136:159735
TI Method for manufacturing a shallow trench for a semiconductor device isolation
IN Kim, Sang Hyun; Kim, Seo Won; Kim, Dae Hee
PA Anam Semiconductor., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000027704	A	20000515	KR 1998-45702	19981029

AB A method is provided to prevent a deterioration of a gate oxide due to an elec. field concn. on trench side wall edges by forming a complete corner **rounding** of shallow trench side wall edges. A pad oxide and a nitride are consecutively formed on the upper of a Si wafer to form a pattern defining an isolation region, and the Si wafer is etched to form a shallow trench. The Si wafer is thermal-oxidized to form a liner oxide on the internal walls of the shallow trench. A thick oxide is deposited on the front side of the Si wafer to **bury** the shallow trench with an oxide. The nitride and the pad oxide are removed. The liner oxide is formed due to a rapid thermal oxidn. process after a N ion injection into the internal walls of the shallow trench.
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for manufg. a shallow trench for a semiconductor device isolation)

L87 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:125516 HCAPLUS
DN 136:159734
TI Method for manufacturing a shallow trench for a semiconductor device isolation
IN Kim, Seo Won
PA Anam Semiconductor., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000027703	A	20000515	KR 1998-45701	19981029

AB A method is provided to enhance device isolation characteristics due to a trench and latch up characteristics by forming a good quality of liner oxide having a complete corner **rounding** of trench edges. A pad oxide and a nitride are consecutively formed on the upper portion of a Si wafer to form a pattern for defining a device isolation region. The Si wafer is etched to form a shallow trench. The Si wafer is thermal-oxidized to form a liner oxide on the internal walls of the shallow trench. A thick oxide is deposited on the front side of the Si wafer to **bury** the shallow trench with the oxide. The thermal oxidn. of the Si wafer is carried out through a rapid thermal process.
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for manufg. a shallow trench for a semiconductor device isolation)

L87 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:54403 HCAPLUS
DN 136:78207
TI Method of forming isolation film of semiconductor device
IN Jung, Yee Sun
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000014700	A	20000315	KR 1998-34244	19980824

AB The presented method improves the characteristics of a device by increasing the radius of a curvature of a top edge of a trench. The method uses the trench technol. to form an isolation film. The method comprises the following steps: forming a pad oxide and a nitride film in sequence on a semiconductor substrate; revealing the substrate in an inactive region by patterning the nitride film and the pad oxide; forming a trench by etching the revealed substrate and **rounding** the trench by the 1st side oxidn.; forming an oxide film having good gap filling capability on the nitride film to **bury** a 1st **rounded** trench; **rounding** the 1st **rounded** trench by the 2nd side oxidn. and performing blanket etching of the oxide film until the nitride film is revealed; and removing the nitride film and the pad oxide, and performing blanket etching of the oxide film until the substrate is revealed. The 2nd side oxidn. is proceeded in the atm. of 1,1,1-trichloroethane and O2. The characteristic of the device is improved by preventing the link in the voltage-current characteristics of the device.

IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method of forming isolation film of semiconductor device)

L87 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:508179 HCAPLUS
DN 133:98155
TI Method to form trench-free **buried** contact in process with shallow **trench isolation** (**STI**) technology
IN Huang, Kuo Ching; Ying, Tse-liang; Tsai, Chia-shiung
PA Taiwan Semiconductor Manufaturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438400000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6093619	A	20000725	US 1998-99809	19980618

AB A new method of forming a **buried** contact junction in a process involving shallow **trench isolation** is described. A 1st Si oxide layer is deposited over a pad oxide layer on the surface of a semiconductor substrate. An opening is etched in the 1st Si nitride and pad oxide layers where they are not covered by a mask. The substrate underlying the opening is etched into to form a shallow trench. An oxide material is deposited over the surface of the 1st Si nitride layer and within the shallow trench and planarized to the surface of the 1st Si nitride layer wherein the oxide material forms a **STI** region. The 1st Si nitride layer is removed whereby the **STI** protrudes above the pad oxide layer. The pad oxide layer is removed whereby the corners of the **STI** above the substrate are also removed. A 2nd Si nitride layer is deposited overlying a sacrificial oxide layer and etched away to leave Si nitride spacers filling in and **rounding** the corners of the **STI**. The sacrificial oxide layer is removed. A gate electrode and source/drain regions are formed in and on the substrate wherein a source/drain is adjacent to the **STI**. The gate electrode and **STI** are covered with an insulating layer. An opening is etched through the insulating layer to the source/drain region wherein the Si nitride spacer at the corner of the **STI** prevents etching of the **STI**. The opening is filled with a conducting layer to complete formation of a contact.

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method to form trench-free **buried** contact in process with shallow **trench isolation** technol.)

L92 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:499815 HCAPLUS
DN 135:69674
TI Method for forming a shallow **trench isolation** using high density plasma-deposited silicon oxynitride
IN Lee, Kong Hean; Chew, Peter
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6258676	B1	20010710	US 1999-431241	19991101

AB A method is presented for forming a shallow **trench isolation** using high d. plasma-deposited Si oxynitride. A pad oxide layer is formed on a semiconductor substrate having an active area and an isolation area and a bottom antireflective coating (BARC) layer is formed over the pad oxide layer. The BARC layer, the pad oxide layer, and the semiconductor substrate are patterned to form a trench having **rounded** corners in the isolation area. A **liner** oxide layer is formed over the semiconductor substrate, and a gap fill layer is formed on the **liner** oxide layer. An important feature of the invention is that the gap fill layer is composed of Si oxynitride formed using a high d. plasma CVD process. A portion of the gap fill layer over the active area can be removed using a reverse trench mask etch, and the gap fill layer is further planarized with a chem. mech. polishing process using the **liner** oxide layer as chem. mech. polishing stop.
IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for forming a shallow **trench isolation** using high d. plasma-deposited silicon oxynitride)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L92 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73494 HCAPLUS
DN 134:124763
TI Method of filling shallow trenches in the manufacture of semiconductor devices
IN Vassiliev, Vladislav; Peidous, Igor
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6180490	B1	20010130	US 1999-318670	19990525

AB This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically to an improved method of filling shallow trenches, in shallow **trench isolation** (**STI**) sub-quarter micron technol. The present method relates to a process for forming trench gap filling with chem. vapor deposited (CVD) SiO2 layers within trenches within substrates employed in integrated circuit fabrication. There is 1st provided a Si substrate having a trench formed therein. There is then formed a SiO2 layer through tetraethylorthosilicate (TEOS) and ozone reaction, at either sub-atm., or atm. pressure, with enhanced surface sensitivity features, which lines the trench providing corner **rounding**. Then there is a thermal oxidn. to form within the trench a thermal SiO2 layer underneath the TEOS-ozone trench SiO2 **liner**. Finally, there is formed on top of the trench a SiO2 layer formed by either low pressure CVD using TEOS, or non-surface-sensitive TEOS ozone CVD, or a high-d. plasma CVD process. All layers are further annealed to form a void-free trench fill.

IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method of filling shallow **trenches** in manuf. of semiconductor devices)

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L92 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:388537 HCAPLUS
DN 133:11783
TI Process for recess-free planarization of shallow **trench isolation** in device fabrication
IN Chang, Jung-Ho; Chen, Hsi-Chuan; Lin, Dahcheng
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6074931	A	20000613	US 1998-187302	19981105

AB An improved and new process for fabricating planarized **isolation trenches**, wherein sharp corners at the top periphery of the trench are eliminated and erosion of insulating material at the edges of **isolation trenches** is suppressed, was developed. The process uses a two layer mask to etch the **isolation trench**, followed by an isotropic etch to recess the 1st layer of the mask. An oxide **liner** is formed in the trench and across the exposed edge of the trench resulting in **rounding** the corners of the trench. Then, a 2nd isotropic etch was used to recess the edge of the 2nd mask layer, so that its opening now is beyond the edge of the trench. An oxide layer is conformally deposited over all exposed surfaces and fills the trench. After CMP to planarize the oxide layer, the remaining oxide fills the trench and, also, extends a small distance beyond the edge of the trench and serves to protect edge of the trench during subsequent etching.
IT **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in process for recess-free planarization of shallow **trench isolation** in device fabrication)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L92 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:388536 HCAPLUS
DN 133:11782
TI Shallow **trench isolation** formation with **trench** wall spacer in device fabrication
IN Kepler, Nick; Bandyopadhyay, Basab; Karlsson, Olov; Wang, Larry; Ibok, Effiong; Lyons, Christopher F.
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6074927	A	20000613	US 1998-87662	19980601

AB A shallow **trench isolation** structure is formed which enables the growth of a high quality gate oxide at the trench edges and protects the field oxide from gouging during post-gate processing, such as during the local interconnect etch, thereby allowing the formation of high-quality implanted junctions. Embodiments include forming a photoresist mask directly on a pad oxide layer which, in turn, is formed on a main surface of a semiconductor substrate or an epitaxial layer on a semiconductor substrate. After masking, the substrate is etched to form a trench, an oxide **liner** is grown in the trench surface, and a polish stop layer is deposited in the trench on the oxide **liner** and on the pad oxide layer. The polish stop layer is then masked to the trench edges, and the polish stop in the trench is anisotropically etched, to remove the polish stop at the bottom of the trenches leaving a portion overlying the side surfaces and edges of the trench on the oxide **liner**. The trench is then filled with an insulating material, the insulating material is planarized, and the polish stop over the pad oxide layer is removed by anisotropic etching. Thus, the oxide **liner** is allowed to grow on the trench edges without the restraint of a polish stop, resulting in a thick, **rounded** oxide on the trench edges. The portion of the polish stop remaining in the trench and on the oxide **liner** at the trench edges serves as a protective spacer, protecting the field oxide from erosion during subsequent processing steps.

IT **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in shallow **trench isolation** formation with **trench** wall spacer in device fabrication)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L94 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:331271 HCAPLUS
DN 134:319690
TI Method to form shallow **trench isolations** with **rounded** corners and reduced trench oxide recess
IN Lim, Chong Wee; Siah, Soh Yun; Lim, Eng Hua; Lee, Kong-Hean; Low, Chun Hui
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6228727	B1	20010508	US 1999-405061	19990927

AB A method of fabricating shallow **trench isolations** was achieved. A semiconductor substrate is provided. A pad oxide layer is grown overlying the semiconductor substrate. A Si nitride layer is deposited. The Si nitride layer and the pad oxide layer are patterned to form a hard mask. The openings in the hard mask correspond to planned trenches in the semiconductor substrate. A SiO2 layer is deposited overlying the Si nitride layer and the semiconductor substrate. The SiO2 layer is anisotropically etched to form sidewall spacers on the inside of the openings of the hard mask. The semiconductor substrate is etched to form the trenches. The sidewall spacers are etched away. The semiconductor substrate is sputter etched to **round** the corners of the trenches. An oxide trench lining layer is grown overlying the semiconductor substrate. A trench fill layer is deposited overlying the Si nitride layer and filling the trenches. The trench fill layer is polished down to the top surface of the Si nitride layer. The Si nitride layer is etched away. The trench fill layer and the pad oxide layer are polished down to the top surface of the semiconductor substrate to complete the shallow **trench isolation**, and the integrated circuit device is completed.

IT **12033-89-5P**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PREP (Preparation); PROC (Process); USES (Uses)
(in method to form shallow **trench isolations** with **rounded** corners and reduced **trench** oxide recess)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L94 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:604638 HCAPLUS
DN 129:253464
TI Method for forming a shallow trench with tapered profile and **round** corners for the application of shallow **trench isolation** (**STI**)
IN Chen, Chao-Cheng; Tsai, C. S.; Yu, C. H.
PA Taiwan Semiconductor Manufacturing, Co., Ltd., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5807789	A	19980915	US 1997-821353	19970320

AB The present invention is a method for forming a shallow trench with tapered profile and **round** corners for the application of shallow **trench isolation** (**STI**). This invention utilizes a multiple-step dry etching process with reduced RF power and increased pressure to etch a shallow trench. This takes advantage of different degree of polymer deposition in different steps by varying the pressure and the RF power. Thus, a shallow trench with tapered profile and **round** corners is achieved.
IT **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etching of, for forming a shallow **trench** with tapered profile and **round** corners for application of shallow **trench isolation** (**STI**) with)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L96 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:380257 HCAPLUS
DN 125:102371
TI Corner-protected shallow **trench isolation** device
IN Mandelman, Jack A.; Machesney, Brian J.; Wong, Hing; Armacost, Michael D.; Pan, Pai-hung
PA International Business Machines Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-00
NCL 257510000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5521422	A	19960528	US 1994-348709	19941202
	US 5741738	A	19980421	US 1996-604283	19960221
PRAI	US 1994-348709		19941202		

AB A semiconductor structure to prevent gate wrap-around and corner parasitic leakage has a semiconductor substrate having a planar surface. A trench is located in the substrate, the intersection of the trench and the surface forms a corner, and a dielec. lines the sidewalls of the trench. A corner dielec. co-aligned with the corner extends a subminimum dimension distance over the substrate from the corner. A FET has a channel with a current path extending parallel to the corner and spaced from the corner by the corner dielec.

IT 7631-86-9, Silica, uses **10043-11-5**, Boron nitride, uses
12033-89-5, Silicon nitride (Si3N4), uses
RL: DEV (Device component use); USES (Uses)
(corner dielec.; for corner-protected shallow **trench isolation** of semiconductor devices)

IT **10043-11-5**, Boron nitride, uses
RL: DEV (Device component use); USES (Uses)
(corner dielec.; for corner-protected shallow **trench isolation** of semiconductor devices)

RN 10043-11-5 HCAPLUS
CN Boron nitride (BN) (8CI, 9CI) (CA INDEX NAME)

B≡N

L98 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:132730 HCAPLUS
DN 130:244862
TI In-situ shallow **trench isolation** etch with clean chemistry
AU Wang, Xikun; Williams, Scott; Padmapani, Nallan; Pan, Shaoher
CS Silicon Etch Division, Applied Materials, Inc., Sunnyvale, CA, 95054, USA
SO IEEE/CPMT International Electronics Manufacturing Technology Symposium, 23rd, Austin, Tex., Oct. 19-21, 1998 (1998), 150-154 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 67HHAB
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB An in-situ hard-mask open and self-clean shallow **trench isolation** (**STI**) etch process with a bromine and fluorine based chem. was developed using an Applied Materials DPS chamber. SEM micrographs from an etched photoresist-patterned wafer show a desired trench profile with **rounded** bottom corners and smooth side walls. Quartz crystal micro-balance (QCM) measurements, coupon tests, and a 1000 wafer extended run demonstrate a clean **STI** process. No dry clean are necessary. The **STI** step used a chem. which balanced oxygen passivation with fluorine based etching. More tapered profiles can be achieved by increasing the O2 flow rate. Also, the side wall passivation and oxidn. improve the bottom corner **rounding**, which is desired to minimize stress and current leakage. Fluorine radicals chem. etch the silicon. With increasing fluorine content, the formation of side wall passivation becomes less pronounced, and therefore the **profile** becomes more **vertical**. This strategy balancing chem. etchants, passivators, energetic ions enables tuning of the profile within wide range. In addn. to chem., the source power and bias power were all varied. The of these parameters on the trench profile angles corner **rounding** and microloading are discussed. The simplicity, cleanliness, and excellent profile performance of the process make it a most promising candidate for sub-micron **STI** manufg.

L102 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:293648 HCAPLUS
DN 134:289043
TI Process of fabricating **buried** diffusion junction for a semiconductor integrated circuit device
IN Peng, Nai-Chen; Yang, Ming-Tzong
PA United Microelectronics Corp., Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438400000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6221731	B1	20010424	US 1998-63022	19980420
PRAI	TW 1998-87100301	A	19980112		

AB A process is disclosed for fabricating **buried** diffusion junction that can be combined with the shallow-**trench isolation** for the memory device cell unit transistor in which both the junction and the isolation can be formed in the same layout. The **buried** diffusion is free from being inadvertently cut apart to cause open-circuiting. A **bird**'s **beak** oxide layer is formed protecting the **buried** diffusion junction region from undesirable etching, thereby preventing from damaging consumption by etching. The **buried** diffusion junctions formed may serve as the source/drain region for the transistor.

IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(process of fabricating **buried** diffusion junction for a semiconductor integrated circuit device)

L102 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:119054 HCAPLUS
DN 116:119054
TI Preparation of **trench-isolated** semiconductor substrates for integrated circuits
IN Morie, Takashi
PA Nippon Telegraph and Telephone Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 03268445	A2	19911129	JP 1990-69070	19900319

AB The process includes: (a) forming a 1st Si-oxide film with **bird beaks** at both ends on a device region of a Si semiconductor substrate; (b) forming a window in the 1st film; (c) forming a trench in the substrate, corresponding to the window; (d) forming a 2nd Si-oxide film on the trench wall; (e) **burying** the trench with polycryst. or amorphous Si such that its top surface comes at the window level; and (f) forming a 3rd Si-oxide film on the **buried** area, which is thinner than the 1st film such that the bottom of the 3rd film is higher than that of the 1st film.
ST **trench isolation** semiconductor substrate integrated circuit
IT Semiconductor materials
(substrates, **trench-isolated**, manuf. of)
IT 7631-86-9, Silicon oxide, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(in manuf. of **trench-isolated** semiconductor substrates for integrated circuits)
IT 7440-21-3P, Silicon, uses
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(trenched **buried** with, semiconductor substrates isolated by, for integrated circuits, manuf. of)

L151 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:213776 HCAPLUS
DN 136:240135
TI Method for forming **trench isolation** regions with **corner rounding** and reduced stress effects in integrated circuits
IN Wu, Shye-Lin
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S., 10 pp., Cont.-in-part of U.S. 5,985,737.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-762
NCL 438431000
CC 76-3 (Electric Phenomena)
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6358818	B1	20020319	US 1999-361447	19990726
	US 5985737	A	19991116	US 1998-34635	19980304
PRAI	US 1998-34635	A2	19980304		

AB The method for forming an isolation region with **rounded corners** includes the following steps. First, a pad layer is formed on a semiconductor substrate and an oxidn. masking layer is formed on the pad layer. The oxidn. masking layer, the pad layer, and the substrate are then patterned to form trenches in the substrate. The pad layer is removed laterally to form undercut structures under the oxidn. masking layer. A doped layer is conformably formed on the oxidn. masking layer, the undercut structures of the pad layer, and the substrate in the trenches. Next, a **thermally** oxidizing step is carried out to oxidize the doped layer to form an oxidized layer conformably on the oxidn. masking layer, the undercut structures of the pad layer, and the substrate in the trenches. A dielec. layer is formed over the substrate to fill up the trenches and cover over the pad layer and the oxidn. masking layer. The dielec. layer is planarized downward to portions of the oxidn. masking layer. Finally, the oxidn. masking layer and the pad layer are removed.

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(nitrogen-doped polysilicon; method for forming **trench isolation** regions with **corner rounding** and reduced stress effects in integrated circuits)

IT 12033-89-5, Silicon nitride, processes
RL: NUU (Other use, unclassified); REM (Removal or disposal); PROC (Process); USES (Uses)
(oxidn. mask; method for forming **trench isolation** regions with **corner rounding** and reduced stress effects in integrated circuits)

151 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:874617 HCAPLUS
DN 136:14132
TI Trench-diffusion **corner rounding** in a shallow-trench (**STI**) process for integrated circuits
IN Liang, Victor; Laparra, Olivier; Rubin, Mark
PA Vlsi Technology, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438424000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6326283	B1	20011204	US 2000-519908	20000307

AB An isolation structure on an integrated circuit is formed using a shallow **trench isolation** process. A layer of **buffer** oxide is formed on a substrate. A layer of nitride is formed on the layer of **buffer** oxide. The layer of nitride and the layer of **buffer** oxide are patterned to form a trench area. An oxidn. of the substrate was performed to provide for **round corners** at a perimeter of the trench area. The substrate is then etched to form a trench within the trench area.
IT Nitrides
RL: DEV (Device component use); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(mask; in trench-diffusion **corner rounding** in shallow-**trench isolation** process for integrated circuits)

L151 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:655107 HCAPLUS
DN 135:203966
TI Fabrication of semiconductor devices by shallow **trench isolation**
IN Sasata, Kazuhiro
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-76
ICS H01L021-316
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001244327	A2	20010907	JP 2000-57174	20000302

AB The title process involves patterning a trench-forming mask on a Si substrate, forming a trench to the substrate, providing an **oxide** film for oxidn.-controlling, and **thermal** oxidizing over the oxidn.-controlling film to give the trench opening a **rounded corner** edge. The **rounded** trench **corner** prevents field concn. on the **corner** to avoid deterioration of withstand voltage in the gate **oxide** film and reverse narrow channel effects.
IT 7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(semiconductor substrate; fabrication of semiconductor devices by shallow **trench isolation**)

L151 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73476 HCAPLUS
DN 134:140377
TI Isotropic assisted dual trench etch
IN Ibok, Effiong E.
PA Advanced Micro Devices, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-336
ICS H01L021-76; H01L021-302; H01L021-461
NCL 438296000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6180466	B1	20010130	US 1997-992843	19971218

AB A method for forming a shallow trench wherein the resulting gate **oxide** layer at the trench edges exhibit high reliability, and to reduce stress at the **corners** and side walls, is described. A shallow **trench isolation** structure having **rounded corners** is formed at edge-**rounding** oxidn. temps. employing a two-step trench etching technique. Isotropic etching is 1st performed, undercutting a pad **oxide** layer and a barrier nitride layer. Subsequently, anisotropic etching is conducted to form the remainder of the trench. The isotropic etch enables the **thermal** oxidn. to form an **oxide** liner with **rounded** edges and reduced stress at relatively low temps., e.g. 900.degree.. or less, even using water vapor as the oxidizing species.

IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(isotropic assisted dual trench etch for stress redn. and formation of shallow trench for formation gate **oxide** with improved reliability)

L151 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:45134 HCAPLUS
DN 134:94401
TI Silicon **corner rounding** by ion implantation for shallow **trench isolation**
IN Fuller, Robert; Davis, Jonathan Philip; Rennie, Michael
PA White Oak Semiconductor Partnership, USA; Infineon Technologies North America Corp.
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438440000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6174787	B1	20010116	US 1999-476725	19991230
WO 2001050501	A2	20010712	WO 2000-US35497	20001228
WO 2001050501	A3	20020321		

W: JP, KR
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

PRAI US 1999-476725 A 19991230
AB A method for **rounding corners** of a Si substrate, in accordance with the present invention, includes forming a plateau on a Si substrate having **corners** at edges of the plateau. A mask is formed on a **top** surface of the plateau, which is recessed back from vertical edges of the plateau to provide exposed horizontal portions. F or Ar dopants are implanted at the **corners** and on the exposed portions, and the substrate is oxidized such that the **corners** become **rounded** providing a gradual transition at the edges of the plateau.
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicon **corner rounding** by ion implantation for shallow **trench isolation**)

L151 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:75156 HCAPLUS
TI Stress-free shallow **trench isolation**
IN Wu, Shye-lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-00
NCL 257506000
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6020621	A	20000201	US 1998-14868	19980128

AB A **trench isolation** in a semiconductor substrate is provided. The **trench isolation** includes a recessed region in the semiconductor substrate. The **trench isolation** also has a first insulator layer lining the recessed region. The first insulator aligns with the semiconductor substrate at edge of the recessed region. The **trench isolation** further includes a second insulator layer filling within the recessed region over the first insulator. As a preferred embodiment, the recessed region can have well **rounded corners** at bottom and abutting **top** surface of the semiconductor substrate. The first insulator has inwardly increased height after the planarization process. The second insulator layer aligns with the first insulator at inner edge of the first insulator. The second insulator layer can also have a **top** plain region.

28may02 13:23:23 User259284 Session D1807.1

File 2:INSPEC 1969-2002/May W4

Set	Items	Description
S1	1582	(ROUND???? OR CURV??? OR CURVILINEAR????)(4N)(INTERFAC????-?? OR CORNER???)
S2	2	'SHALLOW TRENCH ISOLATION CORNER':'SHALLOW TRENCH ISOLATION CORNERS'
S3	1113	STI OR SHALLOW()TRENCH??()ISOLAT??????
S4	18	1AND3
S5	275	CI=(B SS(S)N SS)(S)NE=2
S6	2793	CI=(SI SS(S)N SS)(S)NE=2
S7	2980	S5:S6
S8	1	4AND7
S9	6	S4 AND (TOP OR TOPMOST OR UPPER)
S10	2	S4 AND LINER?
S11	20	S1 AND TRENCH()ISOLAT?????
S12	0	S11 AND (BURY????? OR BURIE???)

9/9/1
DIALOG(R)File 2:INSPEC

6695836 INSPEC Abstract Number: B2000-10-2550E-067
Title: An integrated etch approach as **STI** evolves for the 100 nm regime
Author(s): Lassig, S.; Xu, C.S.; Miller, A.J.; Kamath, S.; Romano, A.; Kudo, T.
Author Affiliation: Lam Res. Corp., Fremont, CA, USA
Journal: Solid State Technology vol.43, no.7 p.157-8, 160, 162
Publisher: PennWell Publishing,
Publication Date: July 2000 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
SICI: 0038-111X(200007)43:7L.157:IEAE;1-W
Material Identity Number: S046-2000-007
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: As **shallow trench isolation** progresses toward the 100 nm regime, numerous technical and manufacturing problems need to be resolved. The work presented here examines the current process parameter envelope, identifies problem areas, and develops an integration scheme that reduces process complexity and cost. The final scheme includes an integrated etch that could process hard mask opening, **top corner rounding** , and silicon trench etch in one pass. It also provides high-density oxide gap-fill that does not require annealing and can be planarized with direct-polish CMP. (10 Refs)
Subfile: B

9/9/2
DIALOG(R)File 2:INSPEC

6658666 INSPEC Abstract Number: B2000-09-2550E-020
Title: Stress minimization of **corner rounding** process during **STI**
Author(s): Olsen, C.S.; Nouri, F.; Rubin, M.; Laparra, O.; Scott, G.
Author Affiliation: VLSI Technol. Inc., San Jose, CA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3881 p.215-23
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3881L.215:SMCR;1-J
Material Identity Number: C574-1999-343
U.S. Copyright Clearance Center Code: 0277-786X/99/$10.00
Conference Title: Microelectronic Device Technology III
Conference Sponsor: SPIE
Conference Date: 22-23 Sept. 1999 Conference Location: Santa Clara, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: For sub 0.25 micron CMOS processes, **shallow trench isolation** (**STI**) is required because of its planarity, high packing density and low junction edge capacitance. After trench etch in the **STI** process, the **top** corner of the trench must be rounded in order to achieve stable device performance, reduce inverse narrow width effects and maintain good gate oxide integrity. Several methods of **rounding** the trench **corners** have been proposed. A post-CMP oxidation step to **round** the **top corner** trench has been shown to consume too much of the silicon active area and may not be suitable for sub 0.18 mu m technologies. Furthermore, the post-CMP oxidation can generate a lot of stress even at high temperatures. It has been shown that a 50 nm radius of curvature provides stable device data and a good gate oxide integrity with minimum consumption of the active area. In this paper, we have shown that this radius can be achieved with minimal stress generation using a properly optimized rapid thermal oxidation before oxide fill. Through both 2D oxidation modeling and experimental verification we have shown that an optimum oxidation temperature can be found when coupled with an undercut of the buffer oxide under the silicon nitride mask. Temperature is the primary parameter for **rounding** of the **top corner** during oxidation while undercut of the buffer oxide lowers the minimum temperature for a given rounding. A 50 nm radius of curvature can be achieved by the balance of the two parameters. This radius of curvature has been shown to suitable for 0.15 micron technology and beyond. (7 Refs)

9/9/3
DIALOG(R)File 2:INSPEC

6589215 INSPEC Abstract Number: B2000-06-2570D-028
Title: New **corner rounding** process for sub-0.15 mu m **shallow trench isolation**
Author(s): Weon-Gil Kim; Jong-Kook Kim; Choong-Bao Kim; Chang-Ju Choi; Jin-Woong Kim; Yil-Wook Kim; Il-Hyun Choi
Author Affiliation: Memory Res. & Dev. Div., Hyundai Electron. Ind. Co. Ltd., Ichon, South Korea
Conference Title: ICVC '99. 6th International Conference on VLSI and CAD (Cat. No.99EX361) p.133-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xvii+620 pp.
ISBN: 0 7803 5727 2 Material Identity Number: XX-2000-00114
U.S. Copyright Clearance Center Code: 0 7803 5727 2/99/$10.00
Conference Title: ICVC'99. 6th International Conference on VLSI and CAD
Conference Sponsor: Korea Semicond. Ind. Assoc.; Hyundai MicroElectron. Co.; IEEK; IEEE Korea Council; SEMI Korea; IEEE Electron Devices Soc.; IEEE Solid-State Circuit
Conference Date: 26-27 Oct. 1999 Conference Location: Seoul, South Korea
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: To obtain a **top corner rounding** in the **Shallow Trench Isolation** (**STI**) process with a hard mask, a new etching spacer and Si soft etching for an useful **top** corner process is evaluated. This technique utilizes the oxide rounding and, thus, effectively suppresses the inverse narrow width effect due to the stress reduction at the **top** corner and the less interface influence between active and field oxide. Also this technique showed no degradation of junction leakage current and less profile micro-loading effect compared with the conventional resist mask process. As a result, it has been found that this technique is very effective for sub-0.15 mu m **STI** formation. (7 Refs)
Subfile: B

10/9/1
DIALOG(R)File 2:INSPEC

6560581 INSPEC Abstract Number: B2000-05-2560R-074
Title: Active corner engineering in the process integration for **shallow trench isolation**
Author(s): Balasubramanian, N.; Johnson, E.; Peidous, I.V.; Shiu Ming-Jr; Sundaresan, R.
Author Affiliation: Dept. of Deep Submicron Integrated Circuits, Inst. of Microelectron., Singapore
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) vol.18, no.2 p.700-5
Publisher: AIP for American Vacuum Soc,
Publication Date: March 2000 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(200003)18:2L.700:ACEP;1-F
Material Identity Number: C067-2000-002
U.S. Copyright Clearance Center Code: 0734-211X/2000/18(2)/700(6)/$15.00
Document Number: S0734-211X(00)01802-3
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The electrical characteristics of metal-oxide-semiconductor field effect transistor devices with **shallow trench isolation** (**STI**) have been studied to evaluate the active corner shaping and the trench-fill dielectric densification techniques. The suppression of corner parasitic transistor effects was observed in the two different corner shaping schemes used. In the first approach, an undercut of pad oxide below the nitride mask defining the active region facilitated corner oxidation during **liner** oxide growth. In the second approach, a high temperature post-chemical mechanical polishing (CMP) oxidation created a **rounded corner**, forming a minibird's beak under the nitride mask edge. Cross-sectional transmission electron microscopy shows that, while the post-CMP oxidation "**rounds**" the **corner**, the pad oxide undercut produces a concave corner profile. Though both approaches improved the subthreshold characteristics of the transistor, the leakage current of field-edge-intensive diodes became very high for post-CMP oxidation. The leakage was also strongly influenced by the annealing ambient during densification of **STI** gap-fill dielectric. An oxidizing ambient resulted in high leakage current whereas a nonoxidizing ambient resulted in low levels of leakage current. The excessive leakage is attributed to the silicon defects generated along the **STI** edge as a result of stress exerted by the gap-fill oxide. Densification in nonoxidizing ambient also helped improve the subthreshold characteristics of the transistors with **STI** fabricated using the pad oxide undercut scheme. (11 Refs)

9/9/4
DIALOG(R)File 2:INSPEC

6507714 INSPEC Abstract Number: B2000-04-2550E-009
Title: **Round**-off of trench **corner** by post-cylindrical molecular pump sidewall oxidation for 0.25 mu m and beyond technologies
Author(s): Chung, Y.S.; Jeon, C.W.; Kim, J.H.; Han, S.K.; Hwang, J.W.; Kim, S.Y.; Lee, J.G.; Hyun, I.S.
Author Affiliation: Hyundai Electron. Ind. Co. Ltd., Kyoungki-do, South Korea
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) vol.18, no.1 p.197-200
Publisher: AIP for American Vacuum Soc,
Publication Date: Jan.-Feb. 2000 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(200001/02)18:1L.197:RTCP;1-8
Material Identity Number: C067-2000-001
U.S. Copyright Clearance Center Code: 0734-211X/2000/18(1)/197(4)/$15.00
Document Number: S0734-211X(90)09101-6
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: A post-cylindrical molecular pump (CMP) sidewall oxidation (PCSWO) has been developed for the **shallow trench isolation** (**STI**) process of 0.25 mu m and beyond complementary metal-oxide-semiconductor technologies. One of the most important factors of **STI** is a **round**-off of trench **top corners** without the loss of active area. The conventional **STI** process usually requires a wall oxidation after trench etch to round off and also an annealing to densify a gap-filled oxide. But PCSWO simplifies the **STI** process by applying sidewall oxidation and annealing simultaneously. The trench was filled with HDP oxide without the conventional wall oxidation after trench etch. After CMP, post-CMP wall oxide was thermally grown to **round** off the trench **corner** at the high temperature of 1100 degrees C. The high temperature wall oxidation has an annealing effect for HDP oxide, which releases a residual film stress. The anomalous subthreshold conduction of the **shallow trench isolated** metal-oxide-semiconductor field effect transistors as the so called "kink effect" due to field crowding at the active edge, was successfully eliminated even at the back bias of +or-5 V. Isolation and diode characteristics of PCSWO-**STI** were comparable to those of the conventional **STI**. Gate oxide reliabilities of PCSWO-**STI** were similar to those of the conventional **STI**. (6 Refs)
Subfile: B
Descriptors: annealing; CMOS integrated circuits; internal stresses;

9/9/5
DIALOG(R)File 2:INSPEC

6327964 INSPEC Abstract Number: B1999-10-2550E-009
Title: Roles of sidewall oxidation in the devices with **shallow trench isolation**
Author(s): Seung-Ho Pyi; In-Seok Yeo; Dae-Hee Weon; Young-Bog Kim; Sahng-Kyoo Lee
Author Affiliation: Semicond. Adv. Res. Div., Hyundai Electron. Ind. Co. Ltd., Kyoungki, South Korea
Journal: IEEE Electron Device Letters vol.20, no.8 p.384-6
Publisher: IEEE,
Publication Date: Aug. 1999 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199908)20:8L.384:RSOD;1-R
Material Identity Number: I338-1999-008
U.S. Copyright Clearance Center Code: 0741-3106/99/$10.00
Document Number: S0741-3106(99)06458-7
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: The effects of sidewall sacrificial and sidewall oxidations on the characteristics of devices with **shallow trench isolation** (**STI**) have been investigated. We found that sidewall sacrificial and sidewall oxidations significantly affected junction leakage and gate oxide integrity (GOI). The sidewall sacrificial oxidation was shown to reduce oxidation-induced stresses and make the trench **top corner** more **rounded**. This reduced stress and more **rounded top corner** led to much improved junction leakage and GOI. These results clearly show that the sidewall sacrificial oxidation is worth using, although it adds complexity to the **STI** process. (14 Refs)
Subfile: B
Descriptors: internal stresses; isolation technology; leakage currents;

9/9/6
DIALOG(R)File 2:INSPEC

5552534 INSPEC Abstract Number: B9705-2550E-173
Title: Correlation between gate oxide reliability and the profile of the trench **top** corner in **Shallow Trench Isolation** (**STI**)
Author(s): Tai-Su Park; Yu Gyun Shin; Han Sin Lee; Moon Han Park; Sang Dong Kwon; Ho Kyu Kang; Young Bum Koh; Moon Yong Lee
Author Affiliation: Semicond. R&D Center, Samsung Electron. Co. Ltd., Kyungki, South Korea
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.96CH35961) p.747-50
Publisher: IEEE, New York, NY, USA
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Abstract: In order to develop a **Shallow Trench Isolation** (**STI**) which does not have trench corner induced degradation of the gate oxide, its integrities were evaluated with **rounded**, non-**rounded top corner**, and an addition of CVD SiO/sub 2/ spacer. In the experiment, we found that the rounded and SiO/sub 2/ spacered **STI** showed the best result meaning no harmful influence of the corner to the gate oxide integrity. Also, etch-back processes of the filled CVD SiO/sub 2/ were modified to eliminate the degradation of the gate oxide by a stress concentration at **top** corner kinks. (6 Refs)
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Si-SiO2-SiN int - SiO2 int - SiN int - O2 int - Si int - N int - O int - SiO2 bin - SiN bin - O2 bin - Si bin - N bin - O bin - Si el (Elements - 1,2,2,3)